(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 504 603 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92102746.2**

(51) Int. Cl.5: **H01J 1/30**, H01J 9/02

(22) Date of filing: **19.02.92**

(30) Priority: **20.02.91 JP 45579/91**
28.02.91 JP 55597/91
13.09.91 JP 234456/91
13.09.91 JP 234457/91

(43) Date of publication of application:
23.09.92 Bulletin 92/39

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IT LI LU NL PT SE

(71) Applicant: **CANON KABUSHIKI KAISHA**
30-2, 3-chome, Shimomaruko, Ohta-ku
Tokyo(JP)

(72) Inventor: **Watanabe, Nobuo, c/o Canon Kabushiki Kaisha**
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo(JP)

Inventor: **Kaneko, Norio, c/o Canon Kabushiki Kaisha**
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo(JP)

Inventor: **Okunuki, Masahiko, c/o Canon Kabushiki Kaisha**
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo(JP)

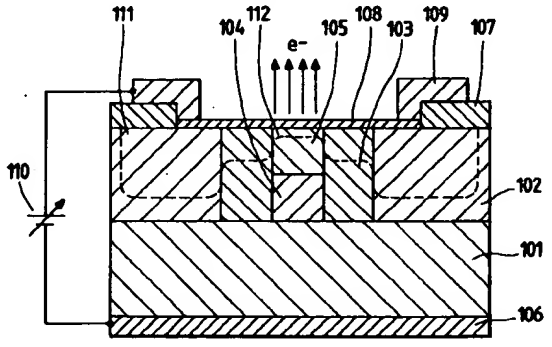
Inventor: **Tsukamoto, Takeo, c/o Canon Kabushiki Kaisha**
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo(JP)

(74) Representative: **Pellmann, Hans-Bernd, Dipl.-Ing. et al**
Patentanwaltsbüro Tiedtke-Bühling-Kinne & Partner, Bavariaring 4
W-8000 München 2(DE)

(54) Semiconductor electron emission device.

(57) On a high density p-type semiconductor substrate, a high density p-type semiconductor region and a p-type semiconductor region 104 for supplying carriers to the high density p-type semiconductor region are disposed in contact, further, a p-type semiconductor region and a low density p-type semiconductor region are disposed outwardly around the high density p-type semiconductor region and the p-type semiconductor region, and on a surface of device, a Schottky electrode which is a metallic film for forming the Schottky barrier junction with the high density p-type semiconductor region is disposed. The density relation between carrier densities of the semiconductor regions is such that high density p-type semiconductor region > p-type semiconductor region > p-type semiconductor region > low density p-type semiconductor region.

FIG. 1



EP 0 504 603 A1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor electron emission device having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, and a high density p-type semiconductor region bringing about the avalanche amplification within the p-type semiconductor under an electrode forming the Schottky barrier junction.

Related Background Art

Conventional semiconductor electron emission devices using the avalanche breakdown mechanism have been known as described in United States Patent No. 4,259,678 and United States Patent No.4,303,930. Such a semiconductor electron emission device is one in which an electron emission portion is fabricated by forming a p-type semiconductor layer and an n-type semiconductor layer on a semiconductor substrate, and depositing cesium on the surface of the n-type semiconductor layer to have a decreased work function of the surface. And a reverse bias voltage is applied across a pn junction formed of the p-type semiconductor layer and the n-type semiconductor layer to cause the avalanche breakdown to make hot electrons, and emit the electrons from the electron emission portion in a direction perpendicular to the surface of the semiconductor substrate.

Besides, there is a semiconductor electron emission device in which a Schottky barrier junction is formed of the p-type semiconductor and a metal material, or the p-type semiconductor and a metallic compound, and a reverse bias voltage is applied across the Schottky barrier junction to cause the avalanche breakdown to make hot electrons and emit the electrons from the electron emission portion in a direction perpendicular to the surface of the semiconductor substrate, as described in Japanese Laid-Open Patent Application No. 1-220328.

With the conventional semiconductor electron device as above described, when the reverse bias voltage is applied across the pn junction or Schottky barrier junction, the avalanche breakdown is caused in the high density p-type semiconductor region where the depletion layer width is formed thinnest, so that electrons having high energy produced therein are emitted from a solid surface to the outside. However, the shape of the depletion layer around the pn junction or Schottky barrier junction has a radius of curvature determined by a carrier density of semiconductor and an applied voltage, and the electric field is more concentrated on the depletion layer than in other regions. Accordingly, the breakdown or leakage of the current around the depletion layer may occur at a lower applied voltage than if the avalanche breakdown occurs in the high density p-type semiconductor region intrinsically required, so that the device characteristics may be deteriorated.

Also, with the electron emission device having the pn junction or Schottky barrier junction, it is possible to increase the radius of curvature around the depletion layer with a decreased carrier density of the p-type semiconductor around the high density p-type semiconductor region where the avalanche breakdown occurs, thereby preventing the breakdown at the lower voltage, but the electrical resistance between an electrode for supplying carriers and the high density p-type semiconductor region where the avalanche breakdown occurs may increase, causing the operating voltage of device to rise, and a problem with the deterioration of device may occur due to the Joule heating.

Thus, with the conventional device, as it is inconvenient to decease the carrier density of the p-type semiconductor region around the high density p-type semiconductor region to the extreme, a guard ring structure of high density n-type semiconductor was formed, concentrically with the high density p-type semiconductor region, within the p-type semiconductor region. Thereby, the depletion layer was formed continuously from the high density p-type semiconductor region outward to the p-type semiconductor region and the high density n-type semiconductor layer so as to have a large radius of curvature in the most outside region, thereby preventing the breakdown or the leakage of current around the depletion layer.

With the device structure of conventional semiconductor electron emission device as above described, a manufacturing process such as the ion injection or the thermal diffusion for forming the ring-like n-type semiconductor region (guard ring structure) at a high density, or a process for forming the ohmic junction electrode to apply the voltage to the guard ring of the high density n-type semiconductor is necessary, in which there is a problem that the manufacturing process is complex.

Also, a wide area for forming the guard ring or its ohmic junction electrode is necessary, and it is difficult to provide a smaller device.

Further, with the conventional semiconductor electron emission device, it is required to supply electrons sufficiently to the high density p-type semiconductor region defining the avalanche amplification, when emitting electrons produced by the avalanche amplification mechanism. However, with the conventional electron emission device, the high density p-type semiconductor region is surrounded

by the p-type semiconductor region having a high resistivity, and thus spaced away from the semiconductor or metallic electrode having a low resistivity for supplying electrons. Accordingly, there is a high resistance between the low resistivity region for supplying electrons and the high density p-type semiconductor region, so that it was difficult to raise the operating speed of the device which is determined by the product RC of its resistance R and a capacitance C in the Schottky barrier junction immediately before the avalanche break-down occurs or in the depletion layer width of the pn junction.

Also, in emitting electrons, the current is concentrated in the high density p-type semiconductor region and the neighborhood thereof, so that the Joule heat is generated in the region having a high resistance, and it was difficult to prevent the breakage or deterioration of device due to the temperature elevation, or the fluctuation in the emission amount of electrons.

SUMMARY OF THE INVENTION

The present invention was achieved in the light of the problems associated with the conventional arts as above described, and aimed to provide a smaller semiconductor electron emission device in which the device structure and the manufacturing process can be simplified, and a higher speed of device in the operation can be attained.

Another object of the present invention is to resolve the above-mentioned conventional problems and provide a semiconductor electron emission device having a high operating speed and with reduced heat generation due to the Joule heating within the device.

There is provided a semiconductor electron emission device, according to the present invention, having an electron emission portion comprised of a Schottky barrier junction between a metallic material or metallic compound material and a semiconductor for emitting electrons from a solid surface, firstly characterized in that the electron emission portion comprising:

a first p-type semiconductor region bringing about the avalanche breakdown by forming the Schottky barrier junction;

a second p-type semiconductor region adjacent to the first p-type semiconductor region for supplying carriers to the first p-type semiconductor region; and

an n-type semiconductor region, located around the first p-type semiconductor region, for forming the Schottky barrier junction with the metal material or metallic compound material as well as forming a pn junction with the first p-type semiconductor region;

wherein the density relation between carrier densities in the first and second p-type semiconductor regions and the n-type semiconductor region, (first p-type semiconductor region) > (second p-type semiconductor region) > (n-type semiconductor region) or (second p-type semiconductor region) ≧ (first p-type semiconductor region) > (n-type semiconductor region).

There is provided a semiconductor electron emission device, according to the present invention, having an electron emission portion comprised of a pn junction between an n-type semiconductor and a p-type semiconductor for emitting electrons from a solid surface, secondly characterized in that the electron emission portion comprising:

a first n-type semiconductor region located on the solid surface, and a first p-type semiconductor region bringing about the avalanche breakdown by forming the pn Junction with the first n-type semiconductor region;

a second p-type semiconductor region adjacent to the first p-type semiconductor region for supplying carriers to the first p-type semiconductor region; and

a second n-type semiconductor region, located around the first p-type semiconductor region, for forming the pn junction with the first p-type semiconductor region;

wherein the density relation between carrier densities in the first and second p-type semiconductor regions and the first and second n-type semiconductor regions,
(first n-type semiconductor region) > (first p-type semiconductor region) > (second p-type semiconductor region) > (second n-type semiconductor region) or (first n-type semiconductor region) > (second p-type semiconductor region) ≧ (first p-type semiconductor region) > (second n-type semiconductor region).

There is provided a semiconductor electron emission device, according to the present invention, having an electron emission portion comprised of a Schottky barrier junction between a metal material or metallic compound material and a semiconductor for emitting electrons from a solid surface, thirdly characterized in that the electron emission portion comprising:

a first p-type semiconductor region bringing about the avalanche breakdown by forming the Schottky barrier junction;

a second p-type semiconductor region located around the first p-type semiconductor region;

a third p-type semiconductor region located around the second p-type semiconductor region; and

a fourth p-type semiconductor region for supplying carriers to the first p-type semiconductor region;

wherein the density relation between carrier densities in the first to fourth p-type semiconductor regions,
(first p-type semiconductor region) > (fourth p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region) or (fourth p-type semiconductor region) ≧ (first p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region).

There is provided a semiconductor electron emission device, according to the present invention, having an electron emission portion comprised of a pn junction between an n-type semiconductor and a p-type semiconductor for emitting electrons from a solid surface, fourthly characterized in that the electron emission portion comprising:

an n-type semiconductor region located on the solid surface, and a first p-type semiconductor region bringing about the avalanche breakdown by forming the pn junction with the n-type semiconductor region;

a second p-type semiconductor region located around the first p-type semiconductor region;

a third p-type semiconductor region located around the second p-type semiconductor region; and

a fourth p-type semiconductor region for supplying carriers to the first p-type semiconductor region;

wherein the density relation between carrier densities in the first to fourth p-type semiconductor regions and the n-type semiconductor region,
(n-type semiconductor region) > (first p-type semiconductor region) > (fourth p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region) or (n-type semiconductor region) > (fourth p-type semiconductor region) ≧ (first p-type semiconductor region) > (second p-type semiconductor regions) > (third p-type semiconductor region).

There is provided a semiconductor electron emission device, according to the present invention, having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, and a high density p-type semiconductor region bringing about the avalanche amplification within the p-type semiconductor under an electrode forming the Schottky barrier junction, fifthly characterized by comprising an electrode for applying the voltage to the Schottky barrier junction electrode on a surface of the high density p-type semiconductor region different from the surface on which the Schottky barrier junction is formed.

There is provided a semiconductor electron emission device, according to the present invention, having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, and a high density p-type semiconductor region bringing about the avalanche amplification within the p-type semiconductor under an electrode forming the Schottky barrier junction, sixthly characterized by comprising a region located in the vicinity of the high density p-type semiconductor region, not in contact with the electrode for forming the Schottky barrier junction, and having a smaller resistivity than the p-type semiconductor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view showing a first example of a semiconductor electron emission device according to the present invention.

Fig. 2 is a view showing one example of an energy band for the semiconductor electron emission device of Schottky barrier junction.

Fig. 3 is a diagram showing one example of the current-voltage characteristics for the semiconductor electron emission device according to the present invention.

Fig. 4 is a diagram showing another example of the current-voltage characteristics for the semiconductor electron emission device according to the present invention.

Fig. 5 is a cross-sectional view showing a second example of a semiconductor electron emission device according to the present invention.

Figs. 6A and 6B are cross-sectional views showing a third example of a semiconductor electron emission device according to the present invention.

Fig. 7 is a cross-sectional view showing a fourth example of a semiconductor electron emission device according to the present invention.

Fig. 8 is a cross-sectional view showing a fifth example of a semiconductor electron emission device according to the present invention.

Figs. 9A and 9B are cross-sectional views showing a sixth example of a semiconductor electron emission deivce according to the present invention.

Fig. 10 is a plan view showing a semiconductor electron emission device in the example of the present invention.

Fig. 11 is a cross-sectional view taken along the line A-A' of Fig. 10.

Fig. 12 is a band diagram for explaining the operation principle of a device according to the present invention.

Fig. 13 is a plan view showing a part of multiple electron emission having semiconductor electron emission devices arranged like the matrix in the example of the present invention.

Fig. 14 is a cross-sectional view taken along the line A-A' of Fig. 13.

Figs. 15A and 15B schematically show a semi-

conductor electron emission device in the example of the present invention, Fig. 15A is a plan view, and Fig. 15B is a cross-sectional view taken along the line A-A' of Fig. 15A.

Figs. 16A and 16B schematically show a semiconductor electron emission device using the pn junction of GaAs semiconductor in the example of the present invention, Fig. 16A is a plan view, and Fig. 16B is a cross-sectional view taken along the line A-A' of Fig. 16A.

Figs. 17A and 17B show the state in which multiple semi-conductor electron emission devices in the example of the present invention are arranged, Fig. 17A is a plan view, and Fig. 17B is a cross-sectional view taken along the line A-A' of Fig. 17A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a semiconductor electron emission device of the present invention, a second p-type semiconductor region having a lower carrier density and a third p-type semiconductor region having a further lower carrier density are formed around a first p-type semiconductor region of high density bringing about the avalanche breakdown. Thereby, it is possible to have a depletion layer the shape of which is thinnest in the first p-type semiconductor region so that the electric field is likely to be concentrated thereon. Accordingly, it is possible to bring about the avalanche breakdown efficiently only in the first p-type semiconductor region. The series resistance value of semiconductor electron emission devices can be decreased by using the fourth p-type semiconductor region having a higher carrier density than the second p-type semiconductor region as the passage for the supply of carriers to the first p-type semiconductor region.

Next, the examples of the present invention will be described with reference to the drawings.

(Example 1)

Fig. 1 is a cross-sectional view showing a semiconductor electron emission device of Schottky barrier junction type in the first example of the present invention.

The semiconductor electron emission device in this example is a Schottky barrier junction device in which a cylindrical high density p-type semiconductor region 105 which is a first p-type semiconductor region and a p-type semiconductor region 104, which is a fourth p-type semiconductor region, for supplying carriers to the high density p-type semiconductor region 105 are disposed in contact with each other on a substantial central portion of a high density p-type semiconductor substrate 101, a p-type semiconductor region 103 which is a second p-type semiconductor region and a low density p-type semiconductor region 102 which is a third p-type semiconductor region are disposed concentrically outwardly around the high density p-type semiconductor region 105 and the p-type semiconductor region 104, and a Schottky electrode 108 which is a metallic film for forming the Schottky barrier junction with the high density p-type semiconductor region 105 is disposed on the surface of the device.

Further, the semiconductor electron emission device in this example is provided with an ohmic junction electrode 106 to the high density p-type semiconductor substrate 101 and an electrode wiring 109 to the Schottky electrode 108 for applying a reverse voltage to the Schottky barrier junction, the reverse voltage being applied from a power source 110.

Note that the electrode wiring 109 is in contact with the Schottky electrode 108 on an insulating film 107 formed on the low density p-type semiconductor region 102 in order to prevent the short circuit with each p-type semiconductor region as previously described. In the figure, 111 shows the shape of a depletion layer end in a state where the reverse voltage is applied, and 112 shows a region where the avalanche breakdown occurs with the application of the reverse voltage.

Here, the electron emission process in a semiconductor electron emission device using the Schottky barrier junction will be described with reference to Fig. 2.

By the application of a reverse bias voltage to a Schottky diode forming the Schottky barrier junction with the p-type semiconductor, the bottom Ec of a conduction band for the p-type semiconductor is at a higher energy level than the vacuum level E_{VAC} for the metal electrode forming the Schottky barrier, so that the avalanche breakdown is brought about. An electron produced by the avalanche breakdown obtains a higher energy than the lattice temperature with the electric field within a depletion layer produced at an interface between semiconductor and metal electrode, and injected from the p-type semiconductor into the metal electrode forming the Schottky barrier junction. The electron having a greater energy than the work function on the surface of metal electrode forming the Schottky barrier junction is discharged into the vacuum. Accordingly, the treatment for the surface of metal electrode to have a lower work function leads to an increase in the emission amount of electrons, as previously described.

A manufacturing process of the semiconductor electron emission device as shown in Fig. 1 will be described specifically by way of an example.

(1) A low density p-type GaAs semiconductor

layer having a beryllium (Be) density of $1x10^{15}cm^{-3}$ or less was grown, 0.6 μm thick, on the high density p-type semiconductor substrate 101 (GaAs) doped with Zn and having a carrier density of $5x10^{18}cm^{-3}$, with the molecular beam epitaxy method (MBE). This low density p-type GaAs semiconductor layer becomes the low density p-type semiconductor region 102 later.

(2) Be ions accelerated to 160keV and 40keV were injected in succession into the region corresponding to the p-type semiconductor region 103, with the focused ion beam (FIB) injection method, so that the Be density is $2x10^{17}cm^{-3}$ substantially uniformly from the surface of the low density p-type GaAs semiconductor layer to the high density p-type semiconductor substrate 101. Also, Be ions were injected into the regions corresponding to the p-type semiconductor region 104 and the high density p-type semiconductor region 105, with the FIB injection method, so that the Be densities are $1x10^{18}cm^{-3}$ and $2x10^{18}cm^{-3}$, respectively.

(3) SiO_2 was deposited as the cap material, about 0.1 μm thick, on the surface of the low density p-type GaAs semiconductor layer having Be ions injected as previously described, with the sputtering method, and then the injection portion was activated with the heat treatment at 850 ° C for 10 seconds.

With the injection process (2) and single heat treatment process (3), as above described, it is possible to form the high density p-type semiconductor region 105, the p-type semiconductor regions 103, 104, and the low density p-type semiconductor region 102 which are the first to fourth p-type semiconductor regions, in which the manufacturing process can be simplified as compared with a conventional device having the high density n-type guard ring and the ohmic junction electrode.

The density relation between carrier densities in the high density p-type semiconductor region 105, the p-type semiconductor regions 103, 104, and the low density p-type semiconductor region 102 is such that high density p-type semiconductor region 105 (first p-type semiconductor region) > p-type semiconductor region 104 (fourth p-type semiconductor region) > p-type semiconductor region 103 (second p-type semiconductor region) > low density p-type semiconductor region 102 (third p-type semiconductor region).

(4) After the SiO_2 film for the heat treatment as previously described was removed, 0.5 μm thick SiO_2 film was formed as the insulating film 107. Also, gold (Au)/chromium (Cr) was vacuum evaporated onto a back surface of the high density p-type semiconductor substrate 101 to form an ohmic junction electrode 106 with the heat treatment at 350 ° C for 5 minutes.

(5) After an opening for the electrode wiring 107 was formed to form the Schottky barrier junction with the normal photolithography, a 8nm thick Schottky electrode 108 was formed within the opening, with the electron beam evaporation and the normal photolithography, by selecting tungsten (W) as the material for forming the Schottky barrier junction to the p-type semiconductor region 103 and the high density p-type semiconductor region 105 composed of p-type GaAs semiconductor.

(6) An electrode wiring 109 was formed, with the normal photolithography, by vacuum evaporating aluminum on a junction portion between the insulating film 107 and the Schottky electrode 108.

The semiconductor electron emission device thus fabricated was installed within a vacuum chamber within which the degree of vacuum was retained at about $1x10^{-7}$Torr, and a voltage of 7V was applied between the ohmic junction electrode 106 and the electrode wiring 109 from a power source 110, so that the electron emisson of about 15pA was observed from the surface of the Schottky electrode 108 above the high density p-type semiconductor region 105. If the applied voltage (device voltage) was sequentially increased up to 10V, the electron emission amount (emission current) was sequentially increased up to about 100pA, as shown in Fig. 3. It is conceived that a depletion layer 111 spreads about 0.04 μm beyond a Schottky barrier interface with the Schottky electrode 108 in the high density p-type semiconductor region 105, when this device voltage is applied. The electric field is most concentrated on an avalanche region 112 of the high density p-type semiconductor region 105, in which region the avalanche breakdown occurs most efficiently.

Also, the electric characteristics are shown in Fig. 4, in which a semiconductor electron emission device, which was fabricated by changing only the Be density of the p-type semiconductor region 104 which is a fourth p-type semiconductor region for supplying carriers to the high density p-type semiconductor region 105 which is a first p-type semiconductor region to $3x10^{18}cm^{-3}$ in the fabrication conditions as above described, was installed within the same vacuum chamber. If a device voltage of 5V was applied to the semiconductor electron emission device from the power source 110, the electron emission (emission current) of about 20pA was observed from the surface of the Schottky electrode 108 above the high density p-type semiconductor region 105. If the device voltage was sequentially increased up to 7V, the emission cur-

rent was also sequentially increased up to about 100pA.

In this example, by providing another electrode via the insulating film on the electrode wiring 109, and setting a potential between the electrode and the electrode wiring 109, it is possible to regulate the flying direction and the kinetic energy of electrons emitted from the electron emission portion.

In this way, it is possible to define the current/voltage characteristics of the semiconductor emission device by changing the carrier density in the p-type semiconductor region 104. Also, it is possible to decrease the series resistance of device and make the operating speed faster by decreasing the resistance of the p-type semiconductor region 104.

In the above examples, GaAs was used as the semiconductor, but other semiconductor materials such as Si, Ge, GaP, AlAs, GaAsP, AlGaAs, SiC, BP, AlN, or diamond are applicable in principle, and particularly, the material of indirect transition type and having a wide band gap is preferable. The semi-insulating region can be fabricated by the use of various endogenic defects or residual impurities within the crystal, and purposely added compensating impurities. When this semi-insulating region is formed, undoped crystal not containing the dopant is also applicable because of its semi-insulating property.

The material for the ohmic junction electrode 106 requires to form the Schottky junction with the p-type semiconductor, and may be, for example, Al, Au or LaB_6, in addition to tungsten (W), as commonly well known. However, since the electron emission efficiency increases with smaller work function of the electrode surface, as previously described, the electron emission efficiency can be increased by coating a material of low work function such as Cs on the surface, when the work function of the material is large.

(Example 2)

Fig. 5 is a cross-sectional view showing a semiconductor electron emission device of pn junction type in the second example of the present invention.

The semiconductor electron emission device in this example is a pn junction device having an electron emission portion in which a cylindrical high density p-type semiconductor region 505 which is a first p-type semiconductor region and a p-type semiconductor region 504, which is a fourth p-type semiconductor region, for supplying carriers to the high density p-type semiconductor region 505 are disposed in contact with each other on a substantial central portion of a high density p-type semiconductor substrate 501, and a p-type semiconductor region 503 which is a second p-type semiconductor region and a low density p-type semiconductor region 502 which is a third p-type semiconductor region are disposed concentrically outwardly around the high density p-type semiconductor region 505 and the p-type semiconductor region 504, and a high density n-type semiconductor region 506 which is an n-type semiconductor region for forming the pn junction with the high density p-type semiconductor region 505 is disposed thereon.

Further, the semiconductor electron emission device in this example is provided with an ohmic junction electrode 507 to the high density p-type semiconductor substrate 501, an ohmic junction electrode 509 to the high density n-type semiconductor region 506, and a low work function coating 510 formed on the high density n-type semiconductor region 506, for applying a reverse voltage to the pn junction, the reverse voltage being applied from a power source 511.

Note that the ohmic junction electrode 509 is in contact with the high density n-type semiconductor region 506 via an insulating film 508 formed along an edge portion of the surface on the low density p-type semiconductor region 502 in order to prevent the short circuit with the low density p-type semiconductor region 502. In the figure, 512 shows the shape of a depletion layer end in a state where the reverse voltage is applied, and 513 shows a region where the avalanche breakdown occurs with the application of the reverse voltage.

A manufacturing process of the semiconductor electron emission device of pn junction type will be described specifically by way of an example.

(1) A low density p-type GaAs semiconductor layer having a Si density of $5 \times 10^{16} cm^{-3}$ or less was grown, 0.6 μm thick, on the high density p-type semiconductor substrate 501 (GaAs) doped with Zn and having a carrier density of 5×10^{18} cm^{-3}, with the MBE method. This low density p-type GaAs semiconductor layer becomes the low density p-type semiconductor region 502 later.

(2) Be ions accelerated to 160keV and 40keV were injected in succession into the region corresponding to the p-type semiconductor region 503, with the FIB method, so that the Be density is $2x10^{17} cm^{-3}$ substantially uniformly from the surface of the low density p-type GaAs semiconductor layer to the high density p-type semiconductor substrate 501. Also, Be ions were injected into the regions corresponding to the p-type semiconductor region 104 and the high density p-type semiconductor region 105, with the FIB injection method, so that the Be densities are $1x10^{18} cm^{-3}$ and $2x10^{18} cm^{-3}$, respectively.

(3) Ions were injected into the region corresponding to the high density n-type semiconductor region 506, so that the Si density is about $1x10^{19}cm^{-3}$. If this high density n-type semiconductor region 506 is formed thick, electron produced with the avalanche breakdown are scattered to lose the energy, causing the electron emission efficiency to decrease. Thus, it is desirable to make the ion injection at a low acceleration voltage, or form the surface with the etching to have a thickness of 20nm or less. The electron emission portion consisting of the pn junction with the high density p-type semiconductor region can be formed by forming this high density n-type semiconductor region 506.

(4) SiO_2 was deposited as the cap material, about 0.1 μm thick, on the surface of the low density p-type GaAs semiconductor layer having ions injected as previously described, with the sputtering method, and then the injection portion was activated with the heat treatment at 850 ° C for 10 seconds.

With the injection processes (2) and (3) and single heat treatment process (4), as above described, it is possible to form the high density p-type semiconductor region 505, the p-type semiconductor regions 503, 504, and the low density p-type semiconductor region 502 which are the first to fourth p-type semiconductor regions, and the high dencity n-type semiconductor region 506 which is the n-type semiconductor region, in which the manufacturing process can be simplified as compared with a conventional device having the high density n-type guard ring.

The density relation between carrier densities in the high density p-type semiconductor region 505, the p-type semiconductor regions 503, 504, and the low density p-type semiconductor region 502 is such that high density n-type semiconductor region 506 (n-type semiconductor region) > high density p-type semiconductor region 505 (first p-type semiconductor region) > p-type semiconductor region 504 (fourth p-type semiconductor region) > p-type semiconductor region 503 (second p-type semiconductor region) > low density p-type semiconductor region 502 (third p-type semiconductor region).

(5) After the SiO_2 film for the heat treatment as previously described was removed, 0.5 μm thick SiO_2 film was formed as the insulating film 508, for which an opening was formed in a range corresponding to the high density n-type semiconductor region 506, with the normal lithography, so as to expose the high density n-type semiconductor region 506. And Au/Cr as the ohmic junction electrode 507 to the high density p-type semiconductor substrate 501, and Au/Ge as the ohmic junction electrode 509 to the high density n-type semiconductor region 506 were vacuum evaporated, respectively, and then the alloying heat treatment was performed at 350 ° C for five minutes.

(6) Cesium (Cs) which was a material of low work function was vacuum evaporated substantially in a monatomic layer on an exposed portion of the high density n-type semiconductor region 506, in the ultra-high vacuum to obtain the low work function coating 510.

The semiconductor electron emission device thus fabricated was installed within a vacuum chamber which was retained at about $1x10^{-11}$Torr or less, and a device voltage of 6V was applied between the ohmic junction electrodes 507 and 509 from the power source 511, so that the electron emission of about 0.1 μA was observed from the surface of the low work function coating 510 (Cs) above the high density p-type semiconductor region 505. In this way, with this example, it is possible to form the semiconductor electron emission device of pn junction type having the same electron emission characteristics as a conventional semiconductor electron emission device, with the simplified manufacturing process.

Also, with this example, like the previous first example, by setting a potential between the ohmic junction electrode 509 and another electrode, it is possible to regulate the flying direction and the kinetic energy of electrons.

(Example 3)

Fig. 6 is a view showing a multi semiconductor electron emission device of Schottky barrier type provided with a plurality of electron emission portions, in a third example of the present invention, in which Fig. 6A is a plan view thereof, and Fig. 6B is a cross-sectional view taken along the line A-A' of Fig. 6A.

The multi semiconductor electron emission device of this example is provided with four electron emission portions 600A, 600B, 600C and 600D, like a matrix, on a high density p-type semiconductor region 602 formed on a semiconductor substrate 601.

Since the electron emission portions 600A, 600B, 600C and 600D all have the same constitution, the electron emission portion 600A will be exemplified.

The electron emission portion 600A has the same constitution as in the previous first example, comprising a high density p-type semiconductor region 606A which is a first p-type semiconductor region, a p-type semiconductor region 605A which is a fourth p-type semiconductor region disposed in

contact with the high density p-type semiconductor region 606A for supplying carriers to the high density p-type semiconductor region 606A, a p-type semiconductor region 604A which is a second p-type semiconductor region located around the high density p-type semiconductor region 606A and the p-type semiconductor region 605A, a low density p-type semiconductor region 603 which is a third p-type semiconductor region located around the p-type semiconductor region 604A, and a Schottky electrode 611A for forming the Schottky barrier junction with the high density p-type semiconductor region 606A.

Further, it is provided with an ohmic junction electrode 609 to the high density p-type semiconductor region 602 and an electrode wiring 610A to the Schottky electrode 611A for applying a reverse voltage to the Schottky barrier junction. The electrode wiring 610A is in contact with the Schottky electrode 611A on an insulating film 608 formed on the low density p-type semiconductor region 603 in order to prevent the short circuit with each p-type semiconductor region as previously described.

The ohmic junction electrode 609 is connected via the high density p-type semiconductor region 607 to the high density p-type semiconductor region 602, and in this example, provided at two positions as shown in Fig. 6A. This ohmic junction electrode 609 is a common electrode to the four electron emission portions 600A, 600B, 600C and 600D.

The Schottky electrode 611A may be connected in common with Schottky electrodes 611B, 611C and 611D (611C, 611D are not shown) of other electron emission portions 600B, 600C and 600D, in which case as the ohmic junction electrode 609 is commonly used, the four electron emission portions 600A, 600B, 600C and 600D are controlled simultaneously for the electron emission operation. On the other hand, when the Schottky electrodes 611A, 611B, 611C and 611D of the electron emission portions 600A, 600B, 600C and 600D are independent of each other, the control for each electron emission portion 600A, 600B, 600C and 600D is allowed.

Further, on the device surface formed with the four electron emission portions 600A, 600B, 600C and 600D constituted as previously described, the portion except for the ohmic junction electrode 609 is covered via a supporting member 612 made of insulating material with a gate 613 composed of metallic film provided on the insulating layer 608. This gate 613 is formed with opening portions 614A, 614B, 614C and 614D at positions corresponding to and upward of the electron emission portions 600A, 600B, 600C and 600D, respectively, whereby electrons emitted from each electron emission portion 600A, 600B, 600C and 600D are passed through the opening portions 614A, 614B, 614C and 614D outward.

A manufacturing process of the multi semiconductor electron emission device will be described specifically by way of an example.

(1) After a reversal pattern was formed on an undoped, semi-insulating semiconductor substrate (GaAs) 601 having a density of impurities of $1x10^{14}cm^{-3}$ or less, with the normal photolithography, the normal ion injection was made so that the Be density was $3x10^{18}cm^{-3}$.

And with the heat treatment at 850 °C for 10 seconds, the stripe-like high density p-type semiconductor region 602 was formed longitudinally in the X direction.

(2) With the MBE method, GaAs was grown, 0.6 μm thick, as the low density p-type semiconductor region 603 having a Be density of $5x10^{15}cm^{-3}$.

(3) Be ions were injected, with the FIB method, into the regions corresponding to the p-type semiconductor regions 604A, 604B, 604C and 604D to have a Be density of $2x10^{17}cm^{-3}$, the regions corresponding to the p-type semiconductor regions 605A, 605B, 605C and 605D to have a Be density of $3x10^{18}cm^{-3}$, and the regions corresponding to the high density p-type semiconductor regions 606A, 606B, 606C and 606D to have a Be density of $2x10^{18}cm^{-3}$. Also, Be ions were injected into the region correponding to the high density p-type semiconductor region 607 to have a Be density of $3x10^{18}cm^{-3}$, with the FIB method.

The MBE growth processes of (1) to (3) and the FIB injection process are carried out without exposure to the atmosphere, because respective apparatuses are connected through vacuum tunnel.

(4) Further, with the heat treatment at 850 °C for 10 seconds, the p-type semiconductor regions 604A, 604B, 604C, 604D, 605A, 605B, 605C, 605D and the high density p-type semiconductor regions 606A, 606B, 606C, 606D, 607 were activated.

(5) After SiO_2 was deposited, 0.2 μm thick, as the insulating film 608, on the low density p-type semiconductor region 603 into which the ion injection was made as previously described, with the normal sputtering method, respective openings were formed, with the normal photolithoetching method, to expose partially the high density p-type semiconductor region 607, the p-type semiconductor regions 604A, 604B, 604C, 604D and the high density p-type semiconductor regions 606A, 606B, 606C, 606D, in order to form the Schottky barrier junction. Au/Cr was vacuum evaporated on the high density p-type semiconductor region 607 to form

the ohmic junction electrode 609 with the heat treatment at 350° C for 5 minutes.

(6) Aluminum (Al) as the electrode wiring 610, and tungsten (W) as the material for forming the Schottky barrier junction to the high density p-type semiconductor regions 606A, 606B, 606C, 606D, were deposited with the electron beam source evaporation 0.5 μm and 8nm thick, respectively, to form the electrode wirings 610A, 610B, 610C, 610D and the Schottky electrodes 611A, 611B, 611C, 611D, with the normal photolithoetching method.

(7) For the supporting member 612 and the gate 613 made of insulating material, SiO_2 and tungsten (W) were sequentially deposited with the vacuum evaporation method, respectively, and the opening portions 614A, 614B, 614C, 614D were formed with the normal photolithoetching method.

With the above processes (1) to (7), the multi semiconductor electron emission device having the four electron emission portions 600A, 600B, 600C, 600D was completed.

In the same way, a multi semiconductor electron emission device having the electron emission portions arranged like a matrix, 20 in the X direction, and 10 in the Y direction, was fabricated, and installed within a vacuum chamber within which the degree of vacuum was at about $1x10^{-7}$ Torr. If a reverse voltage of 7V was applied to the entire area of the electron emission portions, the electron emission of about 20nA in total was observed. Also, by applying a reverse voltage only between arbitrary ohmic junction electrode 609 and arbitrary electrode wiring 610, it was observed that only device located at its intersection emitted electrons. In this way, with this example, it is possible to form an electron emission device having the same electron emission characteristics as a conventional multi semiconductor electron emission device and simply fabricated.

In the semiconductor electron emission device of the present invention, the n-type semiconductor region having a low carrier density is formed around a first p-type semiconductor region having a high density bringing about the avalanche breakdown. Thereby, in a state where the operating voltage is applied, the peripheral portion of a depletion layer formed in the first p-type semiconductor region is continuously adjacent to a depletion layer formed therearound with the pn junction and protected, so that the breakdown or the leakage of current will not occur around the first p-type semiconductor region. Accordingly, it is possible to have a device structure not requiring the guard ring structure for the high density n-type semiconductor, which was conventionally inconvenient from the aspects of a simpler manufacturing process and a smaller device.

Here, by forming the second p-type semiconductor region as the passage of supplying carriers to the first p-type semiconductor region, it is possible to make the series resistance of device an appropriate value. Accordingly, the operating speed can be increased.

(Example 4)

Fig. 7 is a cross-sectional view showing a semiconductor electron emission device of Schottky barrier junction type in the fourth example of the present invention.

The semiconductor electron emission device in this example is a Schottky barrier junction device in which a cylindrical high density p-type semiconductor region 703 which is a first p-type semiconductor region and a p-type semiconductor region 704, which is a second p-type semiconductor region, for supplying carriers to the high density p-type semiconductor region 703 are disposed in contact with each other on a substantial central portion of a high density p-type semiconductor substrate 701, a low density n-type semiconductor region 702 which is an n-type semiconductor region is disposed concentrically outwardly around the high density p-type semiconductor region 703 and the p-type semiconductor legion 704, and a Schottky electrode 708 which is a metallic film for forming the Schottky barrier junction with the high density p-type semiconductor region 703 is disposed on the surface of the device.

Further, the semiconductor electron emission device in this example is provided with an ohmic junction electrode 706 to the high density p-type semiconductor substrate 701 and an electrode wiring 707 to the Schottky electrode 708 for applying a reverse voltage to the Schottky barrier junction, the reverse voltage being applied from a power source 709.

Note that the electrode wiring 707 is in contact with the Schottky electrode 708 on an insulating film 705 formed on the low density n-type semiconductor region 702 in order to prevent the short circuit with each p-type semiconductor region as previously described. In the figure, 710 shows the shape of a depletion layer end in a state where the reverse voltage is applied.

The electron emission process in the semiconductor electron emission device using the Schottky barrier junction of the present invention is the same as described in Fig. 2.

A manufacturing process of the semiconductor electron emission device as shown in Fig. 7 will be described specifically by way of an example.

(1) A low density n-type GaAs semiconductor layer having a silicone (Si) density of

$1x10^{15}cm^{-3}$ or less was grown, 0.6 μm thick, on the high density p-type semiconductor substrate 701 (GaAs) doped with zinc (Zn) and having a carrier density of $5x10^{18}cm^{-3}$, with the molecular beam epitaxy method (MBE). This low density n-type GaAs semiconductor layer becomes the low density n-type semiconductor region 102 later.

(2) Be ions accelerated to 40keV were injected into the region corresponding to the p-type semiconductor region 703, with the focused ion beam (FIB) injection method, so that the Be density is $2x10^{18}cm^{-3}$ substantially uniformly.

(3) Be ions accelerated to 160keV were also injected into the region corresponding to the p-type semiconductor region 704, with the FIB injection method, so that the high density p-type semiconductor substrate 701 is reached and the Be density is $1x10^{18}cm^{-3}$.

(4) SiO_2 was deposited as the insulating material 105, about 0.2 μm thick, with the sputtering method, and then the injection portion was activated with the heat treatment at 850 °C for 10 seconds.

(5) Gold (Au)/chromium (Cr) was vacuum evaporated onto a back surface of the high density p-type semiconductor substrate 701 to form an ohmic junction electrode 706 with the heat treatment at 350 °C for 5 minutes.

(6) Aluminum was vacuum evaporated on the insulating film 705, and the opening portion for the electrode wiring 707 and the insulating film 705 was formed, with the normal photolithography method.

(7) An 8nm thick Schottky electrode 708 was formed within the opening, with the electron beam evaporation and the normal photolithography, by selecting tungsten (W) as the material for forming the Schottky barrier junction to the p-type semiconductor region 704 and the high density p-type semiconductor region 703 made of p-type GaAs semiconductor.

The semiconductor electron emission device thus fabricated was installed within a vacuum chamber within which the degree of vacuum was retained at about $1x10^{-7}$Torr, and a voltage of 7V was applied between the ohmic junction electrode 706 and the electrode wiring 709 from a power source 709, so that the electron emission of about 15pA was observed from the surface of the Schottky electrode 708 above the high density p-type semiconductor region 703. If the applied voltage (device voltage) was sequentially increased up to 10V, the electron emission amount (emission current) was also sequentially increased up to about 100pA, as shown in Fig. 3. It is conceived that a depletion layer 710 spreads about 0.04 μm beyond a Schottky barrier interface with the Schottky electrode 708 in the high density p-type semiconductor region 703, when this device voltage is applied. As the peripheral portion is protected by thick depletion layer formed by the pn junction, the electric field is most concentrated on a portion of the high density p-type semiconductor region 703, in which region the avalanche breakdown occurs efficiently.

Also, the electric characteristics are shown in Fig. 4, in which a semiconductor electron emission device, fabricated by changing only the Be density of the p-type semiconductor region 704 which is a second p-type semiconductor region for supplying carriers to the high density p-type semiconductor region 703 which is a first p-type semiconductor region to $3x10^{18}cm^{-3}$ in the fabrication conditions as above described, was installed within the same vacuum chamber. If a device voltage of 5V was applied to the semiconductor electron emission device from the power source 709, the electron emission (emission current) of about 20pA was observed from the surface of the Schottky electrode 708 above the high density p-type semiconductor region 703. If the device voltage was sequentially increased up to 7V, the emission current was also sequentially increased up to about 100pA.

In this example, by providing another electrode via the insulating film on the electrode wiring 707, and setting a potential between the electrode and the electrode wiring 707, it is possible to regulate the flying direction and the kinetic energy of electrons emitted from the electron emission portion.

In this way, it is possible to define the current/voltage characteristics of the semiconductor emission device by changing the carrier density in the p-type semiconductor region 704. Also, it is possible to decrease the series resistance of the device and make the operating speed faster by decreasing the resistance of the p-type semiconductor region 704.

In the above examples, GaAs was used as the semiconductor, but other semiconductor materials such as Si, Ge, GaP, AlAs, GaAsP, AlGaAs, SiC, BP, AlN, or diamond are applicable in principle, and particularly, the material of indirect transition type and having a wide band gap is preferable.

The material for the ohmic junction electrode 706 requires to form the Schottky barrier junction with the p-type semiconductor, and may be, for example, Al, Au or LaB_6, in addition to tungsten (W), as commonly well known. However, since the electron emission efficiency increases with smaller work function of the electrode surface, as previously described, the electron emission efficiency can be increased by coating a material of low work function such as Cs on the surface, when the work function of the material is large.

(Example 5)

Fig. 8 is a cross-sectional view showing a semiconductor electron emission device of pn junction type in the fifth example of the present invention.

The semiconductor electron emission device in this example is a pn junction device having an electron emission portion in which a cylindrical high density p-type semiconductor region 803 which is a first p-type semiconductor region and a p-type semiconductor region 804, which is a second p-type semiconductor region, for supplying carriers to the high density p-type semiconductor region 803 are disposed in contact with each other on a substantial central portion of a high density p-type semiconductor substrate 801, a low density n-type semiconductor region 802 which is a second n-type semiconductor region is disposed concentrically outwardly around the high density p-type semiconductor region 803 and the p-type semiconductor region 804, and a high density n-type semiconductor region 805 which is a first n-type semiconductor region for forming the pn junction with the high density p-type semiconductor region 803 is disposed thereon.

Further, the semiconductor electron emission device in this example is provided with an ohmic junction electrode 807 to the high density p-type semiconductor substrate 801, an ohmic junction electrode 808 to the high density n-type semiconductor region 805, and a low work function coating 809 formed on the high density n-type semiconductor region 805, for applying a reverse voltage to the pn junction, the reverse voltage being applied from a power source 810.

Note that the ohmic junction electrode 808 is in contact with the high density n-type semiconductor region 805 via an insulating film 806 formed along an edge portion of the surface on the low density p-type semiconductor region 802 in order to prevent the short circuit with the low density n-type semiconductor region 802. In the figure, 811 shows the shape of a depletion layer end in a state where the reverse voltage is applied.

A manufacturing process of the semiconductor electron emission device of pn junction type will be described specifically by way of an example.

(1) A low density n-type GaAs semiconductor layer having a Si density of $5x10^{15}cm^{-3}$ or less was grown, 0.6 μm thick, on the high density p-type semiconductor substrate 801 (GaAs) doped with Zn and having a carrier density of $5x10^{18}cm^{-3}$, with the MBE method. This low density n-type GaAs semiconductor layer becomes the low density n-type semiconductor region 802 later.

(2) Be ions accelerated to 40keV were injected into the region corresponding to the high density p-type semiconductor region 803, with the FIB injection method, so that the Be density is $2x10^{18}cm^{-3}$ substantially uniformly.

(3) Be ions accelerated to 160keV were also injected into the region corresponding to the p-type semiconductor region 804, with the FIB injection method, so that the high density p-type semiconductor substrate 801 is reached and the Be density is $5x10^{17}cm^{-3}$.

(4) Si ions accelerated to 10keV were injected into the region corresponding to the high density n-type semiconductor region 805, with the normal ion injection method, so that the Si density is about $1x10^{19}cm^{-3}$ into a depth of 10nm. As this high density n-type semiconductor region 805 is a region through which electrons produced with the avalanche breakdown in the high density p-type semiconductor region 803 beneath it pass, the energy loss due to the scattering increases if it is formed thick, deteriorating the electron emission efficiency. Thus, it is desirable to have the thickness of 10nm or less by making the ion injection at a low acceleration voltage, or etching the surface after the ion injection. The electron emission portion consisting of the pn junction with the high density p-type semiconductor region can be formed by forming this high density n-type semiconductor regoin 805.

(5) SiO_2 was deposited as the insulating film 806, about 0.2 μm thick, with the sputtering method, and then the injection portion was activated with the heat treatment at 850 °C for 10 seconds.

(6) Au/Cr as the ohmic junction electrode 807 to the high density p-type semiconductor substrate 801, and Au/Ge as the ohmic junction electrode 808 to the high density n-type semiconductor region 805 were vacuum evaporated, respectively, on a back surface of the high density p-type semiconductor substrate 801, the normal photolithoetching was made, and then the alloying heat treatment was performed at 350 °C for five minutes.

(7) Cesium (Cs) which was a material of low work function was vacuum evaporated substantially in a monatomic layer on an exposed portion of the high density n-type semiconductor region 805 in the ultra-high vacuum to obtain the low work function coating 809.

The semiconductor electron emission device thus fabricated was installed within a vacuum chamber which was retained at about $1x10^{-11}$Torr or less, and a device voltage of 6V was applied between the ohmic junction electrodes 807 and 808 from the power source 810, so that the electron emission of about 0.1 μA was observed from the surface of the low work function coating 809 (Cs) above the high density n-type semiconductor

region 805. In this way, with this example, it is possible to form the semiconductor electron emission device of pn junction type having the same electron emission characteristics as a conventional semiconductor electron emission device, with the simplified manufacturing process.

Also, with this example, like the previous fourth example, by setting a potential between the ohmic junction electrode 808 and another electrode, it is possible to regulate the flying direction and the kinetic energy of electrons.

(Example 6)

Fig. 9 is a view showing a multi semiconductor electron emission device of Schottky barrier type provided with a plurality of electron emission portions, in a sixth example of the present invention, in which (a) is a plan view thereof, and (b) is a cross-sectional view taken along the line A-A' of (a).

The multi semiconductor electron emission device of this example is provided with four electron emission portions 900A, 900B, 900C and 900D, like a matrix, on a high density p-type semiconductor region 902 formed on a semiconductor substrate 901.

Since the electron emission portions 900A, 900B, 900C and 900D all have the same constitution, the electron emission portion 900A will be exemplified.

The electron emission portion 900A has the same constitution as in the previous fourth example, comprising a high density p-type semiconductor region 904A which is a first p-type semiconductor region, a p-type semiconductor region 905A which is a second p-type semiconductor region disposed in contact with the high density p-type semiconductor region 904A for supplying carriers to the high density p-type semiconductor region 904A, a low density n-type semiconductor region 903 which is a n-type semiconductor region located around the high density p-type semiconductor region 904A and the p-type semiconductor region 905A, and a Schottky electrode 910A for forming the Schottky barrier junction with the high density p-type semiconductor region 904A.

Further, it is provided with an ohmic junction electrode 908 to the high density p-type semiconductor region 902 and an electrode wiring 909A to the Schottky electrode 910A for applying a reverse voltage to the Schottky barrier junction. The electrode wiring 909A is in contact with the Schottky electrode 910A on an insulating film 907 formed on the low density n-type semiconductor region 903 in order to prevent the short circuit with each p-type semiconductor region as previously described.

The ohmic junction electrode 908 is connected via the high density p-type semiconductor region 906 to the high density p-type semiconductor region 902, and in this example, provided at two positions as shown in Fig. 9A. This ohmic junction electrode 908 is a common electrode to the four electron emission portions 900A, 900B, 900C and 900D.

The Schottky electrode 910A may be connected in common with Schottky electrodes 910B, 910C and 910D (910C, 910D are not shown) of other electron emission portions 900B, 900C and 900D, in which case as the ohmic junction electrode 908 is commonly used, the four electron emission portions 900A, 900B, 900C and 900D are controlled simultaneously for the electron emission operation. On the other hand, when the Schottky electrodes 910A, 910B, 910C and 910D of the electron emission portions 900A, 900B, 900C and 900D are independent of each other, the control for each electron emission portion 900A, 900B, 900C and 900D is allowed.

Further, on the device surface formed with the four electron emission portions 900A, 900B, 900C and 900D constitute as previously described, the portion except for the ohmic junction electrode 908 is covered via a supporting member 911 made of insulating material with a gate 912 composed of metallic film provided on the insulating layer 907. This gate 912 is formed with opening portions 913A, 913B, 913C and 913D at positions corresponding to and upward of the electron emission portions 900A, 900B, 900C and 900D, respectively, whereby electrons emitted from each electron emission portion 900A, 900B, 900C and 900D are passed through the opening portions 913A, 913B, 913C and 913D outward.

A manufacturing process of the multi semiconductor electron emission device will be described specifically by way of an example.

(1) After a reversal pattern was formed on an undoped, semi-insulating semiconductor substrate (GaAs) 901 having a density of impurities of $1x10^{14}cm^{-3}$ or less, with the normal photolithography, the normal ion injection was made so that the Be density was $3x10^{18}cm^{-3}$.

And with the heat treatment at 850° C for 10 seconds, the strike-like high density p-type semiconductor region 902 was formed longitudinally in the X direction.

(2) With the MBE method, GaAs was grown, 0.6 μm thick, as the low density n-type semiconductor region 903 having a Si density of $1x10^{15}cm^{-3}$.

(3) Be ions accelerated to 40keV and 160keV were injected, with the FIB method, into the regions corresponding to the high density p-type semiconductor regions 904A, 904B, 904C and 904D to have a Be density of $2x10^{18}cm^{-3}$, the regions corresponding to the p-type semicon-

ductor regions 905A, 905B, 905C and 905D to have a Be density of $5x10^{17}cm^{-3}$, respectively.
(4) Be ions were injected, with the FIB injection method, into the region corresponding to the high density p-type semiconductor region 906, so that the Be density is $3x10^{18}cm^{-3}$ substantially uniformly from the low density n-type semiconductor region 903 to the high density p-type semiconductor region 902. The MBE growth processes of (1) to (4) and the FIB injection process are carried out without exposure to the atmosphere, because respective apparatuses are connected through vacuum tunnel.

Further, with the heat treatment at 850°C for 10 seconds, the high density p-type semiconductor regions 904A, 904B, 904C and 904D, the p-type semiconductor regions 905A, 905B, 905C and 905D, and high density p-type semiconductor region 906 were activated.
(5) After SiO_2 was deposited, 0.2 μm thick, as the insulating film 907, on the low density p-type semiconductor region 903 into which the ion injection was made as previously described, with the normal sputtering method, respective openings were formed, with the normal photolithoetching method.
(6) Au/Cr was vacuum evaporated on the high density p-type semiconductor region 906 to form the ohmic junction electrode 608 with the heat treatment at 350°C for 5 minutes.
(7) Aluminum (AL) as the electrode wirings 909A, 909B, 909C, 909D, and tungsten (W) as the material for forming the Schottky barrier junction to the high density p-type semiconductor regions 904A, 904B, 904C, 904D, were deposited with the electron beam source evaporation, 0.5 μm and 8nm thick, respectively, to form the electrode wirings 909A, 909B, 909C, 909D and the Schottky electrodes 910A, 910B, 910C, 910D, with the normal photolithoetching method.
(7) For the supporting member 911 and the gate 912 made of insulating material, SiO_2 and tungsten (W) were sequentially deposited with the vacuum evaporation method, respectively, and the opening portions 913A, 913B, 913C, 913D were formed with the normal photolithoetching method.

With the above processes (1) to (8), the multi semiconductor electron emission device having the four electron emission portions 900A, 900B, 900C, 900D were completed.

In the same way, a multi semiconductor electron emission device having the electron emission portions arranged like a matrix, 20 in the X direction, and 10 in the Y direction, was fabricated, and installed within a vacuum chamber within which the degree of vacuum was at about $1x10^{-7}$Torr. If a reverse voltage of 7V was applied to the entire area of the electron emission portions, the electron emission of about 20nA in total was observed. Also, by applying a reverse voltage only between arbitrary ohmic junction electrode 908 and arbitrary electrode wiring 909, it was observed that only device located at its intersection emitted electrons. In this way, with this example, it is possible to form an electron emission device having the same electron emission characteristics as a conventional multi semiconductor electron emission device and simply fabricated.

With the semiconductor electron emission device of the present invention:

(1) A region of small resistivity is provided in the vicinity of the high density p-type semiconductor region bringing about the avalanche breakdown to use it for an electrode for the supply of electrons. Thereby, it is possible to reduce the resistance of electron supply passage to the high density p-type semiconductor region.
(2) The region of small resistivity is formed of, for example, a p-type semiconductor having a high carrier density. Thereby, all the portion except for the metallic electrode for forming the Schottky barrier junction can be formed of the semiconductor, so that the simplified fabrication process can be accomplished without exerting any bad effect on the fundamental characteristics of the device.

That is, according to the present invention, it is possible to make faster the operating speed of the device by providing the region of small resistivity in the vicinity of the high density p-type semiconductor region bringing about the avalanche breakdown. Further, it is possible to avoid the breakage or deterioration of the device due to the Joule heating in the vicinity of the high density p-type semiconductor region bringing about the avalanche breakdown, and reduce the fluctuation in the electron emission amount.

(Example 7)

Figs. 10 and 11 are schematic views showing a semiconductor electron emission device in one example of the present invention. Fig. 10 is a plan view thereof, and Fig. 11 is a cross-sectional view taken along the line A-A' of Fig. 10. In the figure, 1001 is a high density p-type semiconductor substrate, 1002 is a p-type semiconductor layer, 1003 is a high density p-type semiconductor region which is a feature of the present invention, 1004 is a p-type semiconductor layer, 1005 is a ring-like n-type semiconductor region, 1006 is a high density p-type semiconductor region bringing about the avalanche amplification, 1007 is an insulating film, 1008, 1009 are ohmic junction electrodes, respectively, 1010 is a metallic electrode which is a

Schottky barrier junction, 1011 is an end of a depletion layer when a reverse voltage calculated is applied, and 1012 is a power source.

A manufacturing process of the semiconductor electron emission device as shown in Figs. 10 and 11 will be described below.

(1) A p-type GaAs semiconductor layer 1002 doped with Be to have a carrier density of $2x10^{16}cm^{-3}$ was grown on the high density p-type GaAs semiconductor substrate 101 doped with Zn and having a carrier density of $5x10^{18}cm^{-3}$, with the MBE (Molecular Beam Epitaxy) method.

(2) Be ions were injected into the high density p-type semiconductor region 1003, with the FIB (Focused Ion Beam) method, so that the density of impurities is $5x10^{18}cm^{-3}$.

(3) The p-type GaAs semiconductor layer 104 doped with Be was grown to have a carrier density of $2x10^{16}cm^{-3}$ with the MBE method. Then, Si ions were injected to have a density of impurities of $1x10^{19}cm^{-3}$, with the FIB injection method, so that the ring-like n-type semiconductor region 1005 was formed. Further, Be ions were injected to have a density of impurities of $2x10^{18}cm^{-3}$, with the FIB injection method, so that the high density p-type semiconductor region 1006 bringing about the avalanche amplification was formed. After these injection porcesses were completed, the injection portion was activated with the heat treatment at 850 °C for 10 seconds.

(4) SiO_2 was vacuum evaporated as the insulating film 1007, and the opening portion was formed with the normal photolithography.

(5) Au/Ge and Au/Cr were vacuum evaporated on the ring-like n-type semiconductor region 1004 and on a back surface of the high density p-type GaAs semiconductor substrate 1001, respectively, and the ohmic junction electrode 1008 and 1009 were formed with the heat treatment at 400 °C for five minutes.

(6) Further, the 8nm thick electrode 1010 was formed with the electron beam evaporation by selecting W as the material for forming the Schottky barrier junction to the p-type GaAs semiconductor.

The semiconductor electron emission device thus fabricated was installed within a vacuum chamber which was retained at a vacuum of about $1x10^{-7}$Torr, and when a reverse voltage of 5V was applied from the power source 1011, the electron emission of about 0.1nA was observed from the W surface above the high density p-type semiconductor region 1006, and when the applied voltage was further increased up to 10V, the electron emission of about InA was observed. However, the breakage or unstable emission current during the electron emission, which occurred with a conventional device, was not observed. Also, the semiconductor electron emission device realized the fast driving so that the operating speed from the application of electrons to their emission was about 1/4 or less that of the conventional device not having the high density p-type semiconductor region (which was a region having a small resistivity) of the present invention, when the structure and the size were the same. This is because the factor of determining the operating speed of the device depends on the product RC of a resistance R of the region for supplying electrons and a capacitance C of the depletion layer formed in the high density p-type semiconductor region bringing about the avalanche amplification, immediately before the avalanche breakdown occurs, as previously described. In the semiconductor electron emission device, since the capacitance C of the depletion layer is the same as that of the conventional device, but the distance L which is a factor of the resistance R in the region for supplying electrons is shorter, the product RC is smaller, so that the operating speed increases. Also, as the resistance R is smaller, the heat generation due to the Joule heating is suppressed, thereby contributing to the stabilization of the device in increasing the electron emission amount, particularly by raising the applied voltage.

Referring now to Figs. 10 and 11, the operation principle of the semiconductor electron emission device according to the present invention will be described. In this semiconductor electron emission device, applicable semiconductor materials are Si, Ge, GaAs, GaP, AlAs, GaAsP, AlGaAs, SiC, BP, AlN, or diamond in principle, and particularly, the material of indirect transition type and having a wide band gap is preferable. The feature of the present invention is that the distance between the high density p-type semiconductor region 1006 involved in the emission of electrons by bringing about the avalanche amplification as thereinafter described and the high density p-type semiconductor substrate 1001 for supplying electrons to the high density p-type semiconductor region is shorter than the region 1003 of small resistivity. The resistance decreases with shorter distance even if the resistivity of the p-type semiconductor 1004 is the same, so that the operating speed was faster, making it possible to suppress the heat generation due to the Joule heating, as previously described. The material for the electrode 1010 requires to form the Schottky junction with the p-type semiconductor, and may be, for example, Al, Au or LaB_6, in addition to tungsten (W), as commonly well known. However, since the electron emission efficiency increases with smaller work function of the electrode surface, the electron emission efficiency can be increased by coating a material of low work

function such as Cs on the surface, when the work function of the material is large.

Referring now to Fig. 12, the electron emission process in the semiconductor electron emission device of the present invention will be described below. If the reverse bias voltage is applied to the Schottky diode forming the Schottky barrier junction with the p-type semiconductor, the bottom Ec in the conduction band of the p-type semiconductor is at a higher energy level than the vacuum level Evac of the electrode forming the Schottky barrier. Electrons produced with the avalanche amplification obtain the higher energy than at a lattice temperature by the electric field within the depletion layer generated at the semiconductor metal electrode interface, and are injected into the electrode for forming the Schottky barrier junction. The electrons having larger energy than the work function on the electrode surface for forming the Schottky barrier junction are emitted in the vacuum. Accordingly, the treatment of the electrode surface for the lower work function leads to the increase of electron emission amount, as previously described.

(Example 8)

Figs. 13 and 14 are schematic views showing partially a multielectron emission portion, in which semiconductor electron emission devices in another example of the present invention are arranged like a matrix. Fig. 13 is a plan view thereof, and Fig. 14 is a cross-sectional view taken along the line A-A' of Fig. 13. In these figures, 1301 is a semiinsulating semiconductor substrate, 1302 is a strike-like high density p-type semiconductor region longitudinally in the X direction, 1303 is a semi-insulating semiconductor layer, 1304 is a high density p-type semiconductor region having a small resistivity which is a feature of the present invention, 1305 is a semi-insulating semiconductor layer, 1306 is a p-type semiconductor region leading to the high density p-type semiconductor region 1302, 1307 is a ring-like n-type semiconductor region, 1308 is a high density p-type semiconductor regin bringing about the avalanche amplification, 1309 is a high density p-type semiconductor region in contact with the high density p-type semiconductor region 1302, 1310 is an insulator layer, 1311 is an electrode which is an ohmic junction to the n-type semiconductor region 1307, shaped like a ring and disposed lengthwise in the Y direction, 1312 is an ohmic junction electrode to the high density p-type semiconductor region 1309, 1313 is a thin electrode which is a Schottky barrier junction to the p-type semiconductor, 1314 is a supporting member made of insulating material, and 1315 is a gate composed of a metallic film.

A manufacturing process of the semiconductor electron emission device as shown in Figs. 13 and 14 will be described.

(1) Be ions were injected on the semi-insulating GaAs semiconductor substrate 1301 having a carrier density of $1x10^{12}cm^{-3}$ or less so as to have a carrier density of $5x10^{18}cm^{-3}$, with the FIB (Focused Ion Beam) method, so that a stripe-like high density p-type semiconducotr region 1302, lengthwise in the X direction, was formed.

(2) With the MBE (Molecular Beam Epitaxy) method, the semi-insulating GaAs semiconductor layer 1303 having a carrier density of $1x10^{13}cm^{-3}$ or less was grown. Then, Be ions were injected into the high density p-type semiconductor region 1304 to have a density of impurities of $5x10^{18}cm^{-3}$, with the FIB injection method. Further, with the MBE method, the semi-insulating GaAs semiconductor layer 1305 was grown to have a carrier density of $1x10^{13}cm^{-3}$ or less.

(3) Be ions accelerated to 40keV, 140keV and 200keV were injected successively into the p-type semiconductor region 1306, respectively, with the FIB injection method, so that the density of impurities of $2x10^{16}cm^{-3}$ is obtained substantially uniformly from the surface to the high density p-type GaAs semiconductor layer 1302. Then, Be ions were also injected into the high density p-type semiconductor region 1309, like 1306, with the FIB injection, so that the carrier density is $5x10^{18}cm^{-3}$ or greater. Then, Si ions were injected to have a density of impurities of $1x10^{19}cm^{-3}$, with the FIB injection method, so that the ring-like n-type semiconductor region 1307 was formed. Further, Be ions were injected to have a density of impurities of $2x10^{18}cm^{-3}$ with the FIB injection method, so that the high density p-type semiconductor region 1308 bringing about the avalanche amplification was formed.

The FIB injection processes and the MBE growth processes of (1) to (4) are carried out without exposure to the atmosphere, because respective apparatuses are connected through vacuum tunnel. After these injection processes were completed, the injection portion was activated with the heat treatment at 850°C for 10 seconds.

(5) AlN (aluminum nitride) was vacuum evaporated as the insulating film 1310, and the opening was formed, with the normal photolithoetching method.

(6) Au/Ge and Au/Cr were vacuum evaporated on the ring-like n-type semiconductor region 1307 and on the high density p-type semiconductor region 1309, respectively, and the ohmic junction electrodes 1311 and 1312 were formed

with the heat treatment at 400 ° C for 5 minutes.

(7) The 8nm thick electrode 1313 was formed, with the electron beam evaporation method, by selecting W as the material for forming the Schottky barrier junction to the p-type GaAs semicoductor.

(8) SiO_2 and W were deposited sequentially, with the vacuum evaporation method, as the supporting member 1314 and the gate 1315 made of insulating material, respectively, which were then formed with the normal photolithography method.

The multi semiconductor electron emission device having the electron emission portions thus fabricated arranged like a matrix, 20 in the X direction, and 15 in the Y direction, was installed within a vacuum chamber which was evacuated to a vacuum of about $1x10^{-7}$Torr. If a reverse bias voltage of 7V was applied to the entire area of the multi device, the electron emission of about 60nA in total was observed. The operating speed of this device was substantially the same as that of single device. In the driving for a long time, there was no breakage or deterioration of the device or no fluctuation in the electron emission amount.

With the semiconductor electron emission device of the present invention:

(1) A semiconductor region of small resistivity or metallic electrode is provided in direct contact with a surface of the high density p-type semiconductor region bringing about the avalanche breakdown, which is different from the surface bringing about the avalanche breakdown. Thereby, it is possible to reduce the resistance of electron supply passage to the avalanche breakdown portion.

(2) The region of small resistivity is formed with the ion injection method. Thereby, it is possible to control the resistance in that region easily and precisely.

Accordingly, according to the present invention, it is possible to make faster the operating speed of the device by providing the semiconductor region of small resistivity or metallic electrode for supplying electrons in direction contact with the high density p-type semiconductor region bringing about the avalanche breakdown. Further, it is possible to avoid the breakage or deterioration of the device due to the Joule heating in the vicinity of the high density p-type semiconductor region bringing about the avalanche amplification, and reduce the fluctuation in the electron emission amount.

(Example 9)

Fig. 15 shows schematically a semiconductor electron emission device in one example of the present invention, in which Fig. 15A is a plan view thereof, and Fig. 15B is a cross-sectional view taken along the line A-A' of Fig. 15A. In the figure, 1501 is a high density p-type semiconductor substrate, 1502 is a p-type semiconductor layer, 1503 is a high density p-type semiconductor region, 1504 is a p-type semiconductor layer, 1505 is a ring-like n-type semiconductor region, 1506 is a high density p-type semiconductor region bringing about the avalanche amplification, 1507 is an insulating film, 1508, 1509 are ohmic junction electrodes, respectively, 1510 is a metallic electrode which is a Schottky barrier junction, 1511 is an end of a depletion layer when a reverse voltage calculated is applied, and 1512 is a power source.

A manufacturing process of the semiconductor electron emission device as shown in Fig. 15 will be described below.

(1) A p-type GaAs semiconductor layer 1502 doped with Be to have a carrier density of $2x10^{16}cm^{-3}$ was grown on the high density p-type GaAs semiconductor substrate 1501 doped with Zn and having a carrier density of $5x10^{18}cm^{-3}$, with the MBE (Molecular Beam Epitaxy) method.

(2) Be ions were injected into the high density p-type semiconductor region 1503, with the FIB (Focused Ion Beam) method, so that the density of impurities is $5x10^{18}cm^{-3}$. This region 1503 in intended to reduce the resistivity, and a higher carrier density is generally preferable. After the injection, the activation of the injection portion and the recovery of crystal were carried out with the heat treatment at 850 ° C for 10 seconds.

(3) The p-type GaAs semiconductor layer 104 doped with Be was grown to have a carrier density of $2x10^{16}cm^{-3}$ with the MBE method. Then, Si ions were injected to have a density of impurities of $1x10^{19}cm^{-3}$, with the FIB injection method, so that the ring-like n-type semiconductor region 1505 was formed. Further, Be inns were injected to have a density of impurities of $2x10^{18}cm^{-3}$, and reach the high density p-type semiconductor region 1503, with the FIB injection method, so that the high density p-type semiconductor region 1506 bringing about the avalanche amplification was formed. After these injection processes were completed, the injection portion was activated with the heat treatment at 850 ° C for 10 seconds.

(4) SiO_2 was vacuum evaporated as the insulating film 1507, and the opening portion was formed with the normal photolithography.

(5) Au/Ge and Au/Cr were vacuum evaporated on the ring-like n-type semicondutor region 1504 and on a back surface of the high density p-type GaAs semiconductor substrate 1501, respectively, and the ohmic junction electrode 1508 and

1509 were formed with the heat treatment at 400 ° C for five minutes.

(6) Further, the 8nm thick electrode 1510 was formed with the electron beam evaporation by selecting W as the material for forming the Schottky barrier junction to the p-type GaAs semiconductor.

The semiconductor electron emission device (Fig. 15) thus fabricated was installed within a vacuum chamber which was retained at a vacuum of about $1x10^{-7}$Torr, and when a reverse bias voltage of 5V was applied from the power source 1511, the electron emission of about 0.InA was observed from the W surface above the high density p-type semiconductor region 1506, and when the applied voltage was further increased up to 10V, the electron emission of about InA was observed. However, the breakage or unstable emission current during the electron emission, which occurred with a conventional device, was not observed. Also, the semiconductor electron emission device realized the fast driving so that the operating speed from the application of electrons to their emission was about 1/4 or less that of the conventional device not having the high density p-type semiconductor region 1503 of the present invention, when the structure and the size were the same. This is because the factor of determining the operating speed of the device depends on the product RC of a resistance R of the region for supplying electrons and a capacitance C of the depletion layer formed in the high density p-type semiconductor region bringing about the avalanche amplification, immediately before the avalanche breakdown occurs, as previously described. In this semiconductor electron emission device, since the capacitance C of the depletion layer is the same as that of the conventional device, but the resistance R in the region for supplying electrons is shorter, the product RC is smaller, so that the operating speed increases. Also, as the resistance R is smaller, the heat generation due to the Joule heating is suppressed, thereby contributing to the stabilization of the device in increasing the electron emission amount, particularly by raising the applied voltage.

Referring now to Figs. 12 and 15, the operation principle of the semiconductor electron emission device according to the present invention will be described. In Fig. 15, applicable semiconductor materials are Si, Ge, GaAs, GaP, AlAs, GaAsP, AlGaAs, SiC, BP, AlN, or diamond in principle, and particularly, the material of indirect transition type and having a wide band gap is preferable. The feature of the present invention is that the resistance between the high density p-type semiconductor region 1506 involved in the emission of electrons by bringing about the avalanche amplification as thereinafter described and the high density p-type semiconductor substrate 1501 for supplying electrons to the high density p-type semiconductor region is smaller. Thereby, the operating speed of the device was faster, making it possible to suppress the heat generation due to the Joule heating, as previously described. The material for the electrode 1510 requires to form the Schottky barrier junction with the p-type semiconductor, and may be, for example, Al, Au or LaB_6, in addition to tungsten (W), as commonly well known. However, since the electron emission efficiency increases with smaller work function of the electrode surface, the electron emission efficiency can be increased by coating a material of low work function such as Cs on the surface, when the work function of the material is large.

Referring now to Fig. 12, the electron emission process in the semiconductor electron emission device using the Schottky barrier junction of the present invention will be described below. If the reverse bias voltage is applied to the Schottky diode forming the Schottky barrier junction with the p-type semiconductor, the bottom Ec in the conduction band of the p-type semiconductor is at a higher energy level than the vacuum level Evac of the electrode forming the Schottky barrier. Electrons produced with the avalanche amplification obtain the higher energy than at a lattice temperature by the electric field within the depletion layer generated at the semiconductor-metal electrode interface, and are injected into the electrode for forming the Schottky barrier junction. The electrons having large energy than the work function on the electrode surface for forming the Schottky barrier junction are emitted in the vacuum. Accordingly, the treatment of the electrode surface for the lower work function leads to the increase of electron emission amount, as previously described.

(Example 10)

Fig. 16 shows schematically a semiconductor electron emission device using the pn junction in one example of the present invention, in which Fig. 16A is a plan view thereof, and Fig. 16B is a cross-sectional view taken along the line A-A' of Fig. 16A. In the figure, 1601 is a high density p-type semiconductor substrate, 1602 is a p-type semiconductor layer, 1603 is a high density p-type semiconductor region, 1604 is a p-type semiconductor layer, 1605 is a ring-like n-type semiconductor region, 1606 is a high density p-type semiconductor region bringing about the avalanche amplification, 1607 is a high density n-type semiconductor layer forming the pn junction with the p-type semiconductor 1604 and the high density p-type semiconductor region 1606, 1608 is an insulating film, 1609, 1610 are ohmic junction electrodes, respectively, 1611 is a

thin film of low work function material, 1612 is an end of a depletion layer when a reverse bias voltage calculated is applied, and 1613 is a power source.

A manufacturing process of the semiconductor electron emission device as shown in Fig. 16 will be described below.

(1) A p-type GaAs semiconductor layer 1602 doped with Be to have a carrier density of $2x10^{16}cm^{-3}$ was grown on the high density p-type GaAs semiconductor substrate 1601 doped with Zn and having a carrier density of $5x10^{18}cm^{-3}$, with the MBE (Molecular Beam Epitaxy) method.

(2) Be ions were injected into the high density p-type semiconductor region 1603, with the FIB (Focused Ion Beam) method, so that the density of impurities is $5x10^{18}cm^{-3}$.

(3) The p-type GaAs semiconductor layer 1604 doped with Be was grown to have a carrier density of $2x10^{16}cm^{-3}$ with the MBE method. Then, Si ions were injected to have a density of impurities of $1x10^{19}cm^{-3}$, with the FIB injection method, so that the ring-like n-type semiconductor region 1605 was formed. Further, Be ions were injected to have a density of impurities of $2x10^{18}cm^{-3}$, and reach the high density p-type semiconductor region 1603, with the FIB injection method, so that the high density p-type semiconductor region 1606 bringing about the avalanche amplification was formed.

(4) Si ions were injected as the thin high density n-type semiconductor layer 1607, with the normal ion injection method, so that the density of impurities is $8x10^{18}cm^{-3}$ into a depth of 10nm. As this high density n-type semiconductor layer is a region through which electrons produced with the avalanche breakdown beneath it pass, the energy loss due to scattering increases if it is formed thick, remarkably deteriorating the electron emission efficiency. Accordingly, to form the thin high density n-type semiconductor layer, it is necessary to make the ion injection at a low acceleration voltage, or make the surface thinner with the etching after the ion injection.

(5) After these injection processes were completed, the injection portion was activated with the heat treatment at 850° C for 10 seconds.

(6) SiO_2 was vacuum evaporated as the insulating film 1608, and then the opening portion was formed with the normal photolithography.

(7) Au/Ge and Au/Cr were vacuum evaporated on the ring-like n-type semiconductor region 1605 and on a back surface of the high density p-type GaAs semiconductor substrate 1601, respectively, and the ohmic junction electrode 1609 and 1610 were formed with the heat treatment at 400° C for 5 minutes.

(8) Cesium (Cs) as the thin film 1611 made of a material of low work function was vacuum evaporated substantially in a monatomic layer.

The semiconductor electron emission device of pn junction type thus fabticated was installed within a vacuum chamber which was retained at a vacuum of about $1x10^{-9}$Torr or less, and when a reverse bias voltage of 7V was applied from the power source 1611, the electron emission of about InA was observed. However, the breakage or unstable emission current during the electron emission, which occurred with a conventional device, was not observed. Also, the semiconductor electron emission device realized the fast driving so that the operating speed from the application of electrons to their emission was about 1/4 or less that of the conventional device not having the high density p-type semiconductor region 1603 of the present invention, when the structure and the size were the same.

(Example 11)

Fig. 17 shows schematically a multi electron emission portion; in part, in which semiconductor electron emission devices in another example of the present invention are arranged like a matrix. Fig. 17A is a plan view thereof, and Fig. 17B is a cross sectional view taken along the line A-A' of Fig. 17A. In these figures, 1701 is a semi-insulating semiconductor substrate, 1702 is a stripe-like high density p-type semiconductor region, disposed lengthwise in the X direction, 1703 is a semi-insulating semiconductor layer, 1704 is a high density p-type semiconductor region, 1705 is a semi-insulating semiconductor layer, 1706 is a p-type semiconductor region leading to the high density p-type semiconductor region 1702, 1707 is a ring-like n-type semiconductor region, 1708 is a high density p-type semiconductor region bringing about the avalanche amplification, 1709 is a high density p-type semiconductor region in contact with the high density p-type semiconductor region 1702, 1710 is an insulator layer 1711 is an electrode which is an ohmic junction to the n-type semiconductor region 1707, shaped like a ring and disposed lengthwise in the Y direction, 1712 is an ohmic junction electrode to the high density p-type semiconductor region 1709, 1713 is a thin electrode which is a Schottky barrier junction to the p-type semiconductor, 1714 is a supporting member made of insulating material, and 1715 is a gate composed of a metallic film.

A manufacturing process of the semiconductor electron emission device as shown in Fig. 17 will be described.

(1) Be ions were injected into the semiinsulating GaAs semiconductor substrate 1701 having a

carrier density of $1x10^{12}cm^{-3}$ or less so as to have a carrier density of $5x10^{18}cm^{-3}$, with the FIB method, so that a stripe-like high density p-type semiconductor region 1702, lengthwise in the X direction, was formed.

(2) With the MBE method, the semi-insulating GaAs semiconductor layer 1703 having a carrier density of $1x10^{13}cm^{-3}$ or less was grown. Then, Be ions were injected into the high density p-type semiconductor region 1704 to have a density of impurities of $8x10^{18}cm^{-3}$, with the FIB injection method. Further, with the MBE method, the semi-insulating GaAs semiconductor layer 1705 was grown to have a carrier density of $1x10^{13}cm^{-3}$ or less.

(3) Be ions accelerated to 40keV, 140keV and 200keV were injected successively into the p-type semiconductor region 1706, with the FIB injection method, so that the density of impurities of $2x10^{16}cm^{-3}$ is obtained substantially uniformly from the surface to the high density p-type GaAs semiconductor layer 1702. Then, Be ions were also injected into the high density p-type semiconductor region 1709, like 1706, with the FIB injection, so that the carrier density is $5x10^{18}cm^{-3}$ or greater. Then, Si ions were injected to have a density of impurities of $1x10^{19}cm^{-3}$, with the FIB injection method, so that the ring-like n-type semicoductor region 1707 was formed. Further, Be ions were injected to have a density of impurities of $2x10^{18}cm^{-3}$ with the FIB injection method, so that the high density p-type semiconductor region 1708 bringing about the avalanche amplification was formed.

The FIB injection processes and the MBE growth processes of (1) to (4) are carried out without exposure to the atmosphere, because respective apparatuses are connected through vacuum tunnel. After these injection processes were completed, the injection portion was activated with the heat treatment at 850 °C for 10 seconds.

(5) AlN (aluminum nitride) was vacuum evaporated as the insulating film 1710, and the opening was formed, with the normal photolithography method.

(6) Au/Ge and Au/Cr were vacuum evaporated on the ring-like n-type semiconductor region 1707 and on the high density p-type semiconductor region 1709, respectively, and the ohmic junction electrodes 1711 and 1712 were formed with the heat treatment at 400 °C for 5 minutes.

(7) The 8nm thick electrode 1713 was formed, with the electron beam evaporation method, by selecting W as the material for forming the Schottky barrier junction to the p-type GaAs semiconductor.

(8) SiO_2 and W were deposited sequentially, with the vacuum evaporation method, as the supporting member 1714 and the gate 1715 made of insulating material, respectively, which were then formed with the normal photolithography method.

The multi semiconductor electron emission device having the electron emission portions thus fabricated arranged like a matrix, 20 in the X direction, and 15 in the Y direction, was installed within a vacuum chamber which was evacuated to a vacuum of about $1x10^{-7}$Torr. If a reverse bias voltage of 7V was applied to the entire area of the multi device, the electron emission of about 60nA in total was observed. The operating speed of this device was substantially the same as that of single device. In the driving for a long time, there was no breakage or deterioration of the device or no fluctuation in the electron emission amount.

The present invention can exhibit the following effects owing to the constitution as above described.

(1) Since the second p-type semiconductor region of a low density and the third p-type semiconductor region of a further lower density are formed outside the first p-type semiconductor region having a high carrier density, the shape of depletion layer can be made such that the electric field is most concentrated on the first p-type semiconductor region. Thereby, the avalanche breakdown will occur efficiently only in the first p-type semiconductor region, and the guard ring structure and its ohmic junction electrode which were provided in the conventional arts as previously described are unnecessary, so that the device structure and the manufacturing process can be simplified.

(2) Since the series resistance of the device can be smaller by providing a higher carrier density in the fourth p-type semiconductor region for supplying carriers to the first p-type semiconductor region than in the second p-type semiconductor region located around the first p-type semiconductor region, it is possible to provide a semiconductor electron emission device having a faster operating speed.

(3) Since the high density p-type semiconductor region defining the avalanche amplification and the high density semiconductor region or metallic electrode for supplying electrons are directly in contact, the product RC between a resistance R of the region leading to the depletion layer bringing about the avalanche amplification and a capacitance C of the depletion layer can be reduced, so that the operating speed of the device determined by the product RC can be incresaed. Also, as the resistance R can be reduced, it is possible to aviod the heat genera-

tion or deterioration of the device due to the Joule heating therein or suppress the fluctuation in the electron emission amount.

On a high density p-type semiconductor substrate, a high density p-type semiconductor region and a p-type semiconductor region 104 for supplying carriers to the high density p-type semiconductor region are disposed in contact, further, a p-type semiconductor region and a low density p-type semiconductor region are disposed outwardly around the high density p-type semiconductor region and the p-type semiconductor region, and on a surface of device, a Schottky electrode which is a metallic film for forming the Schottky barrier junction with the high density p-type semiconductor region is disposed. The density relation between carrier densities of the semiconductor regions is such that high density p-type semiconductor region > p-type semiconductor region > p-type semiconductor region > low density p-type semiconductor region.

Claims

1. A semiconductor electron emission device, having an electron emission portion comprised of a Schottky barrier junction between a metal material or metallic compound material and a semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

   a first p-type semiconductor region bringing about the avalanche breakdown by forming said Schottky barrier junction;

   a second p-type semiconductor region located around said first p-type semiconductor region;

   a third p-type semiconductor region located around said second p-type semiconductor region; and

   a fourth p-type semiconductor region for supplying carriers to said first p-type semiconductor region;

   wherein the density relation between carrier densities of said first to fourth p-type semiconductor regions is such that (first p-type semiconductor region) > (fourth p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region).

2. The semiconductor electron emission device according to claim 1, characterized in that said first p-type semiconductor region and said fourth p-type semiconductor region of said electron emission portion are in contact.

3. The semiconductor electron emission device according to claim 1, characterized in that an electrode for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

4. The semiconductor electron emission device according to claim 1, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

5. The semiconductor electron emission device according to claim 1, characterized in that on a surface of said electron emission portion made of a metal material or metallic compound material forming the Schottky barrier junction, a material having a different work function from said metal material or metallic compound material is deposited.

6. The semiconductor electron emission device according to claim 1, characterized in that said electron emission portion is formed on a semiconductor substrate.

7. The semiconductor electron emission device according to claim 1, characterized in that a plurality of electron emission portions are provided on the same substrate.

8. The semiconductor electron emission device according to claim 7, characterized in that said substrate is a semiconductor substrate.

9. The semiconductor electron emission device according to claim 7, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

10. The semiconductor electron emission device according to claim 1, characterized in that said first to fourth p-type semiconductor regions of the electron emission portion are formed with the ion injection method.

11. A semiconductor electron emission device, having an electron emission portion comprised of a Schottky barrier junction between a metal material or metallic compound material and a semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

    a first p-type semiconductor region bringing about the avalanche breakdown by forming said Schottky barrier junction;

a second p-type semiconductor region located around said first p-type semiconductor region;

a third p-type semiconductor region located around said second p-type semiconductor region; and

a fourth p-type semiconductor region for supplying carriers to said first p-type semiconductor region;

wherein the density relation between carrier densities of said first to fourth p-type semiconductor regions is such that (fourth p-type semiconductor region) ≥ (first p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region).

12. The semiconductor electron emission device according to claim 11, characterized in that said first p-type semiconductor region and said fourth p-type semiconductor region of said electron emission portion are in contact.

13. The semiconductor electron emission device according to claim 11, characterized in that an electrode for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a device surface.

14. The semiconductor electron emission device according to claim 11, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of a device surface.

15. The semiconductor electron emission device according to claim 11, characterized in that on a surface of said electron emission portion made of a metal material or metallic compound material forming the Schottky barrier junction, material having a different work function from said metal material or metallic compound material is deposited.

16. The semiconductor electron emission device according to claim 11, characterized in that said electron emission portion is formed on a semiconductor substrate.

17. The semiconductor electron emission device according to claim 11, characterized in that a plurality of electron emission portions are provided on the same substrate.

18. The semiconductor electron emission device according to claim 17, characterized in that said substrate is a semiconductor substrate.

19. The semiconductor electron emission device according to claim 17, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

20. The semiconductor electron emission device according to claim 11, characterized in that said first to fourth p-type semiconductor regions of the electron emission portion are formed with the ion injection method.

21. A semiconductor electron emission device, having an electron emission portion comprised of a pn junction between an n-type semiconductor and a p-type semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

an n-type semiconductor region located on said solid surface;

a first p-type semiconductor region bringing about the avalanche breakdown by forming said pn junction with said n-type semiconductor region;

a second p-type semiconductor region located around said first p-type semiconductor region;

a third p-type semiconductor region located around said second p-type semiconductor region; and

a fourth p-type semiconductor region for supplying carriers to said first p-type semiconductor region;

wherein the density relation between carrier densities of said first to fourth p-type semiconductor regions and said n-type semiconductor region is such that

(n-type semiconductor region) > (first p-type semiconductor region) > (fourth p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region).

22. The semiconductor electron emission device according to claim 21, characterized in that said first p-type semiconductor region and said fourth p-type semiconductor region of said electron emission portion are in contact.

23. The semiconductor electron emission device according to claim 21, characterized in that an electron for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

24. The semiconductor electron emission device

according to claim 21, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

25. The semiconductor electron emission device according to claim 21, characterized in that on a surface of said n-type semiconductor region in said electron emission portion, a material having a different work function is deposited.

26. The semiconductor electron emission device according to claim 21, characterized in that said electron emission portion is formed on a semiconductor substrate.

27. The semiconductor electron emission device according to claim 21, characterized in that a plurality of electron emission portions are provided on the same substrate.

28. The semiconductor electron emission device according to claim 27, characterized in that said substrate is a semiconductor substrate.

29. The semiconductor electron emission device according to claim 27, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

30. The semiconductor electron emission device according to claim 21, characterized in that said first to fourth p-type semiconductor regions and said n-type semiconductor region are formed with the ion injection method.

31. A semiconductor electron emission device, having an electron emission portion comprised of a pn junction between an n-type semiconductor and a p-type semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

an n-type semiconductor region located on said solid surface for forming said pn junction;

a first p-type semiconductor region bringing about the avalanche breakdown by forming said pn junction with said n-type semiconductor region;

a second p-type semiconductor region located around said first p-type semiconductor region;

a third p-type semiconductor region located around said second p-type semiconductor region; and

a fourth p-type semiconductor region for supplying carriers to said first p-type semiconductor region;

wherein the density relation between carrier densities of said first to fourth p-type semiconductor regions and said n-type semiconductor region is such that

(n-type semiconductor region) > (fourth p-type semiconductor region) ≥ (first p-type semiconductor region) > (second p-type semiconductor region) > (third p-type semiconductor region).

32. The semiconductor electron emission device according to claim 31, characterized in that said first p-type semiconductor region and said fourth p-type semiconductor region of said electron emission portion are in contact.

33. The semiconductor electron emission device according to claim 31, characterized in that an electrode for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

34. The semiconductor electron emission device according to claim 31, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of solid surface.

35. The semiconductor electron emission device according to claim 31, characterized in that on a surface of said n-type semiconductor region in said electron emission portion, a material having a different work function is deposited.

36. The semiconductor electron emission device according to claim 31, characterized in that said electron emission portion is formed on a semiconductor substrate.

37. The semiconductor electron emission device according to claim 31, characterized in that a plurality of electron emission portions are provided.

38. The semiconductor electron emission device according to claim 37, characterized in that said substrate is a semiconductor substrate.

39. The semiconductor electron emission device according to claim 37, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

40. The semiconductor electron emission device

according to claim 31, characterized in that said first to fourth p-type semiconductor regions and said n-type semiconductor region are formed with the ion injection method.

41. A semiconductor electron emission device, having an electron emission portion comprised of a Schottky barrier junction between a metal material or metallic compound material and a semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

a first p-type semiconductor region bringing about the avalanche breakdown by forming said Schottky barrier junction;

a second p-type semiconductor region, located in contact with said first p-type semiconductor region, for supplying carriers to have first p-type semiconductor region; and

an n-type semiconductor region, located around said frist p-type semiconductor region, for forming a pn junction with said first p-type semiconductor region, as well as forming said Schottky barrier junction with said metal material or metallic compound material;

wherein the density relation between carrier densities of said first and second p-type semiconductor regions and said n-type semiconductor region is such that
(first p-type semiconductor region) > (second p-type semiconductor region) > (n-type semiconductor region).

42. The semiconductor electron emission device according to claim 41, characterized in that an electrode for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

43. The semiconductor electron emission device according to claim 41, cahracterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of solid surface.

44. The semiconductor electron emission device according to claim 41, characterized in that on a surface of metal material or metallic compound material forming the Schottky barrier junction in said electron emission portion, a material having a different work function from said metal material or metallic compound material is deposited.

45. The semiconductor electron emission device according to claim 41, characterized in that said electron emission portion is formed on a semiconductor substrate.

46. The semiconductor electron emission device according to claim 41, characterized in that a plurality of electron emission portions are provided on the same substrate.

47. The semiconductor electron emission device according to claim 46, characterized in that said substrate is a semiconductor substrate.

48. The semiconductor electron emission device according to claim 46, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

49. The semiconductor electron emission device according to claim 41, characterized in that said first and second p-type semiconductor regions and said n-type semiconductor region in said electron emission portion are formed with the ion injection method.

50. A semiconductor electron emission device, having an electron emission portion comprised of a Schottky barrier junction between a metal material or metallic compound material and a semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

a first p-type semiconductor region bringing about the avalanche breakdown by forming said Schottky barrier junction;

a second p-type semiconductor region, located in contact with said first p-type semiconductor region, for supplying carriers to said first p-type semiconductor region; and

an n-type semiconductor region, located around said first p-type semiconductor region, for forming a pn junction with said first p-type semiconductor region, as well as forming said Schottky barrier junction with said metal material or metallic compound material;

wherein the density relation between carrier densities of said first and second p-type semiconductor regions and said n-type semiconductor region is such that
(second p-type semiconductor region) ≥ (first p-type semiconductor region) > (n-type semiconductor region).

51. The semiconductor electron emission device according to claim 50, characterized in that an electrode for defining the flying direction of electron emitting from said electron emission portion is provided in the vicinity of a device

surface.

52. The semiconductor electron emission device according to claim 50, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of a device surface.

53. The semiconductor electron emission device according to claim 50, characterized in that on a surface of metal material or metallic compound material forming the Schottky barrier junction in said electron emission portion, a material having a different work function from said metal material or metallic compound material is deposited.

54. The semiconductor electron emission device according to claim 50, characterized in that said electron emission portion is formed on a semiconductor substrate.

55. The semiconducotr electron emission device according to claim 50, characterized in that a plurality of electron emission portions are provided on the same substrate.

56. The semiconductor electron emission device according to claim 55, characterized in that said substrate is a semiconductor substrate.

57. The semiconductor electron emission device according to claim 55, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

58. The semiconductor electron emission device according to claim 50, characterized in that said first and second p-type semiconductor regions and said n-type semiconductor region in said electron emission portion are formed with the ion injection method.

59. A semiconductor electron emission device, having an electron emission portion comprised of a pn junction between an n-type semiconductor and a p-type semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

a first n-type semiconductor region located on said solid surface;

a first p-type semiconductor region bringing about the avalanche breakdown by forming said pn junction with said first n-type semiconductor region;

a second p-type semiconductor region, located in contact with said first p-type semiconductor region, for supplying carriers to said first p-type semiconductor region; and

a second n-type semiconductor region, located around said first p-type semiconductor region, for forming the pn junction with said first p-type semiconductor region;

wherein the density relation between carrier densities of said first and second p-type semiconductor regions and said first and second n-type semiconductor regions is such that (first n-type semiconductor region) > (first p-type semiconductor region) > (second p-type semiconductor region) > (second n-type semiconductor region).

60. The semiconductor electron emission device according to claim 59, characterized in that an electrode for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

61. The semiconductor electron emission device according to claim 59, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

62. The semiconductor electron emission device according to claim 59, characterized in that on a surface of the first n-type semiconductor region in said electron emission portion, a material having a different work function is deposited.

63. The semiconductor electron emission device according to claim 59, characterized in that said electron emission portion is formed on a semiconductor substrate.

64. The semiconductor electron emission device according to claim 59, characterized in that a plurality of electron emission portions are provided on the same substrate.

65. The semiconductor electron emission device according to claim 64, characterized in that said substrate is a semiconductor substrate.

66. The semiconductor electron emission device according to claim 64, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

67. The semiconductor electron emission device according to claim 59, characterized in that said first and second p-type semiconductor regions and said first and second n-type semiconductor regions are formed with the ion injection method.

68. A semiconductor electron emission device, having an electron emission portion comprised of a pn junction between an n-type semiconductor and a p-type semiconductor for emitting electrons from a solid surface thereof, characterized in that said electron emission portion comprising:

a first n-type semiconductor region located on said solid surface;

a first p-type semiconductor region bringing about the avalanche breakdown by forming said pn junction with said first n-type semiconductor region;

a second p-type semiconductor region, located in contact with said first p-type semiconductor region, for supplying carriers to said first p-type semiconductor region; and

a second n-type semiconductor region, located around said first p-type semiconductor region, for forming the pn junction with said first p-type semiconductor region;

wherein the density relation between carrier densities of said first and second p-type semiconductor regions and said first and second n-type semiconductor regions is such that (first n-type semiconductor region) > (second p-type semiconductor region) ≧ (first p-type semiconductor region) > (second n-type semiconductor region).

69. The semiconductor electron emission device according to claim 68, characterized in that an electrode for defining the flying direction of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

70. The semiconductor electron emission device according to claim 68, characterized in that an electrode for defining the kinetic energy of electron emitted from said electron emission portion is provided in the vicinity of a solid surface.

71. The semiconductor electron emission device according to claim 68, characterized in that on a surface of the first n-type semiconductor region in said electron emission portion, a material having a different work function is deposited.

72. The semiconductor electron emission device according to claim 68, characterized in that said electron emission portion is formed on a semiconductor substrate.

73. The semiconductor electron emission device according to claim 68, characterized in that a plurality of electron emission portions are provided on the same substrate.

74. The semiconductor electron emission device according to claim 73, characterized in that said sbustrate is a semiconductor substrate.

75. The semiconductor electron emission device according to claim 73, characterized in that a plurality of electron emission portions are electrically independent to emit electrons separately.

76. The semiconductor electron emission device according to claim 68, characterized in that said first and second p-type semiconductor regions and said first and second n-type semiconductor regions are formed with the ion injection method.

77. A semiconductor electron emission device, having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, and a high density p-type semiconductor region bringing about the avalanche amplification within said p-type semiconductor under an electrode forming the Schottky barrier junction, characterized by comprising a region located in the vicinity of said high density p-type semiconductor region, not in contact with said electrode for forming said Schottky barrier junction, and having a smaller resistivity than said p-type semiconductor.

78. A semiconductor electron emission device, having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, a high density p-type semiconductor region bringing about the avalanche amplification within said p-type semiconductor under an electrode forming the Schottky barrier junction, and an n-type semiconductor region formed around the high density p-type semiconductor region, characterized by comprising a region located in the vicinity of said high density p-type semiconductor region, not in contact with said electrode for forming said Schottky barrier junction and said n-type semiconductor regin, and having a smaller resistivity than said p-type semiconductor.

79. The semiconductor electron emission device according to claim 77, wherein it has a laminated structure in which a p-type semiconductor forming the Schottky barrier junction is formed on a second p-type semiconductor having a smaller resistivity than said p-type semiconductor, characterized in that a region located in the vicinity of said high density p-type semiconductor region bringing about the avalanche amplification, not in contact with said electrode for forming said Schottky barrier junction and said n-type semiconductor region, and having a smaller resistivity than said p-type semiconductor forming said Schottky barrier junction, is formed at a position in contact with said second p-type semiconductor having the smaller resistivity within said p-type semiconductor forming said Schottky barrier junction.

80. The semiconductor electron emission device according to claim 78, wherein it has a laminated structure in which a p-type semiconductor forming the Schottky barrier junction is formed on a second p-type semiconductor having a smaller resistivity than said p-type semiconductor, characterized in that a region located in the vicinity of said high density p-type semiconductor region bringing about the avalanche amplification, not in contact with said electrode for forming said Schottky barrier junction and said n-type semiconductor region, and having a smaller resistivity than said p-type semiconductor forming said Schottky barrier junction, is formed at a position in contact with said second p-type semiconductor having the smaller resistivity within said p-type semiconductor forming said Schottky barrier junction.

81. The semiconductor electron emission device according to claim 79, characterized in that a region located in the vicinity of said high density p-type semiconductor region bringing about the avalanche amplification, not in contact with said electrode for forming said Schottky barrier junction, and having a smaller resistivity than said p-type semiconductor forming said Schottky barrier junction, is in contact with said p-type semiconductor layer having the smaller resistivity.

82. The semiconductor electron emission device according to claim 79, characterized in that a region located in the vicinity of said high density p-type semiconductor region bringing about the avalanche amplification, not in contact with said electrode for forming said Schottky barrier junction, and having a smaller resistivity than said p-type semiconductor forming said Schottky barrier junction, is formed with the ion junction method.

83. The semiconductor electron emission device according to claim 79, characterized in that a region located in the vicinity of said high density p-type semiconductor region bringing about the avalanche amplification, not in contact with said electrode for forming said Schottky barrier junction, and having a smaller resistivity than said p-type semiconductor forming said Schottky barrier junction, is a p-type semiconductor.

84. A semiconductor electron emission device, having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, and a high density p-type semiconductor region bringing about the avalanche amplification within said p-type semiconductor under an electrode forming the Schottky barrier junction, characterized by comprising an electrode for applying the voltage to said Schottky barrier junction electrode on a surface of said high density p-type semiconductor region different from the surface on which said Schottky barrier function is formed.

85. A semiconductor electron emission device, having a Schottky barrier junction on the surface of a p-type semiconductor which is a substrate, a high density p-type semiconductor region bringing about the avalanche amplification within said p-type semiconductor under an electrode forming the Schottky barrier function, and an n-type semiconductor region formed around said high density p-type semiconductor region, characterized by comprising an electrode for applying the voltage to said Schottky barrier junction electrode on a surface of said high density p-type semiconductor region different from the surface on which said Schottky barrier junction is formed.

86. The semiconductor electron emission device according to claim 84, wherein it has a laminated structure in which a p-type semiconductor forming the Schottky barrier junction is formed on a p-type semiconductor layer having a smaller resistivity than said p-type semiconductor, characterized in that said high density p-type semiconductor region bringing about the avalanche amplification is formed in contact with said p-type semiconductor layer having the smaller resistivity.

87. The semiconductor electron emission device according to claim 85, wherein it has a laminated structure in which a p-type semiconductor forming the Schottky barrier junction is formed on a p-type semiconductor layer having a smaller resistivity than said p-type semiconductor, characterized in that said high density p-type semiconductor region bringing about the avalanche amplification is formed in contact with said p-type semiconductor layer having the smaller resistivity.

88. A semiconductor electron emission device, having a pn junction on the surface of a p-type semiconductor which is a substrate, and a high density p-type semiconductor region bringing about the avalanche amplification within said p-type semiconductor under a thin n-type semiconductor layer forming the pn junction, characterized by comprising an electrode for applying the voltage to said pn junction electrode on a surface of said high density p-type semiconductor region different from the surface on which said pn junction is formed.

89. A semiconductor electron emission device, having a pn junction on the surface of a p-type semiconductor which is a substrate, a high density p-type semiconductor region bringing about the avalanche amplification within said p-type semiconductor under a thin n-type semiconductor layer forming the pn junction, and an n-type semiconductor region formed around said high density p-type semiconductor region, characterized by comrpising an electrode for applying the voltage to said pn junction electrode on a surface of said high density p-type semiconductor region different from the surface on which said pn junction is formed.

90. The semiconductor electron emission device according to claim 88, wherein it has a laminated structure in which a p-type semiconductor forming the pn junction is formed on a p-type semiconductor layer having a smaller resistivity than said p-type semiconductor, characterized in that said high density p-type semiconductor region bringing about the avalanche amplification is formed in contact with said p-type semiconductor layer having the smaller resistivity.

91. The semiconductor electron emission device according to claim 89, wherein it has a laminated structure in which a p-type semiconductor forming the pn junction is formed on a p-type semiconductor layer having a smaller resistivity than said p-type semiconductor, characterized in that said high density p-type semiconductor region bringing about the avalanche amplification is formed in contact with said p-type semiconductor layer having the smaller resistivity.

92. The semiconductor electron emission device acccording to claim 84, characterized in that said high density p-type semiconductor region bringing about the avalanche breakdown is formed with the ion injection method.

93. The semiconductor electron emission device according to claim 85, characterized in that said high density p-type semiconductor region bringing about the avalanche breakdown is formed with the ion injection method.

94. The semiconductor electron emission device according to claim 88, characterized in that said high density p-type semiconductor region bringing about the avalanche breakdown is formed with the ion injection method.

95. The semiconductor electron emission device according to claim 89, characterized in that said high density p-type semiconductor region bringing about the avalanche breakdown is formed with the ion injection method.

FIG. 1

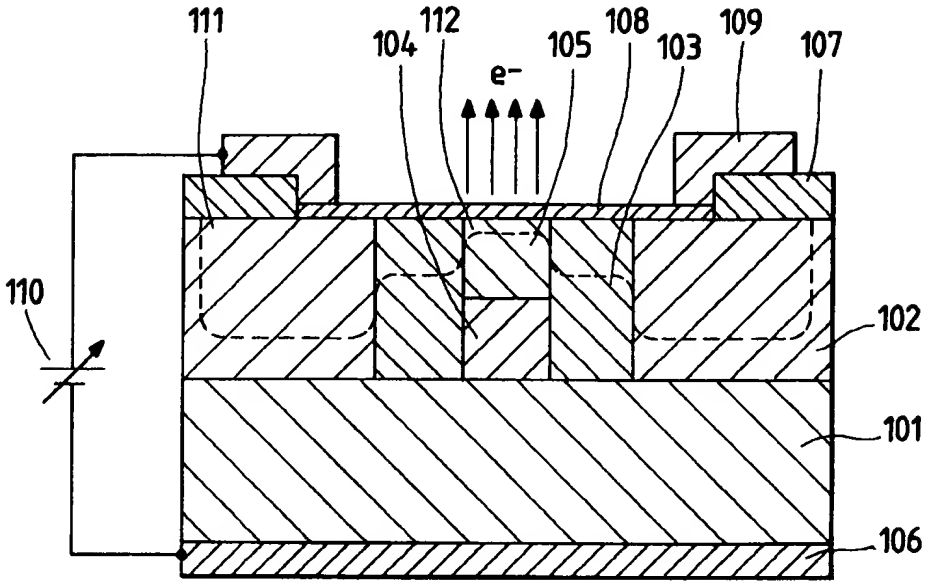

111
112
104
105
108
103
109
107
e-
110
102
101
106

FIG. 2

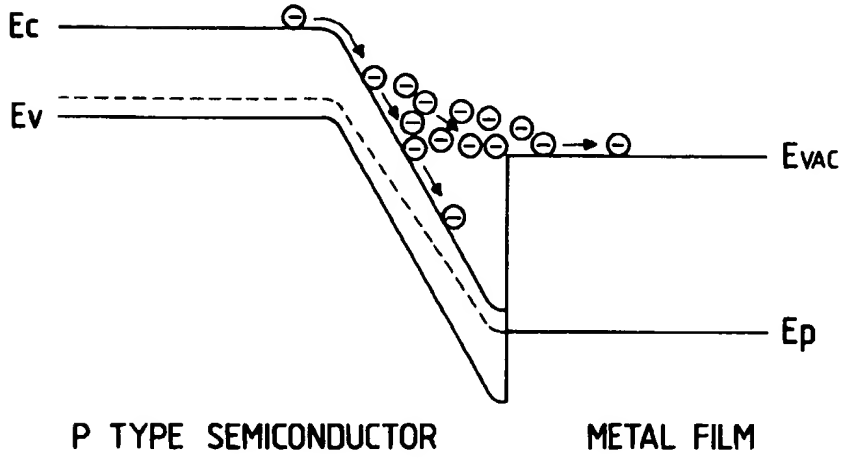

Ec
Ev
EVAC
Ep
P TYPE SEMICONDUCTOR
METAL FILM

FIG. 3

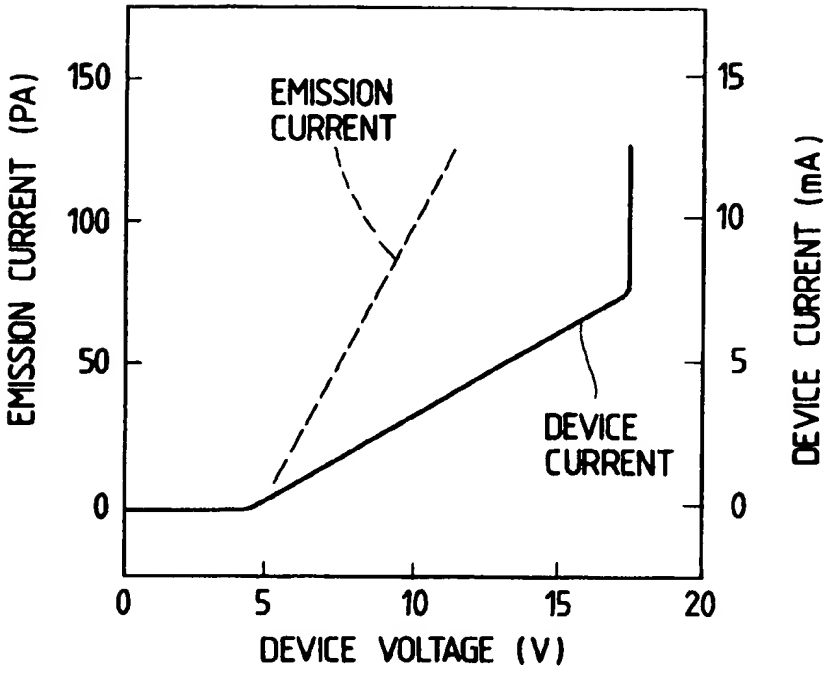

EMISSION CURRENT (PA)
150
100
50
0
EMISSION CURRENT
DEVICE CURRENT
15
10
5
0
DEVICE CURRENT (mA)
0
5
10
15
20
DEVICE VOLTAGE (V)

FIG. 4

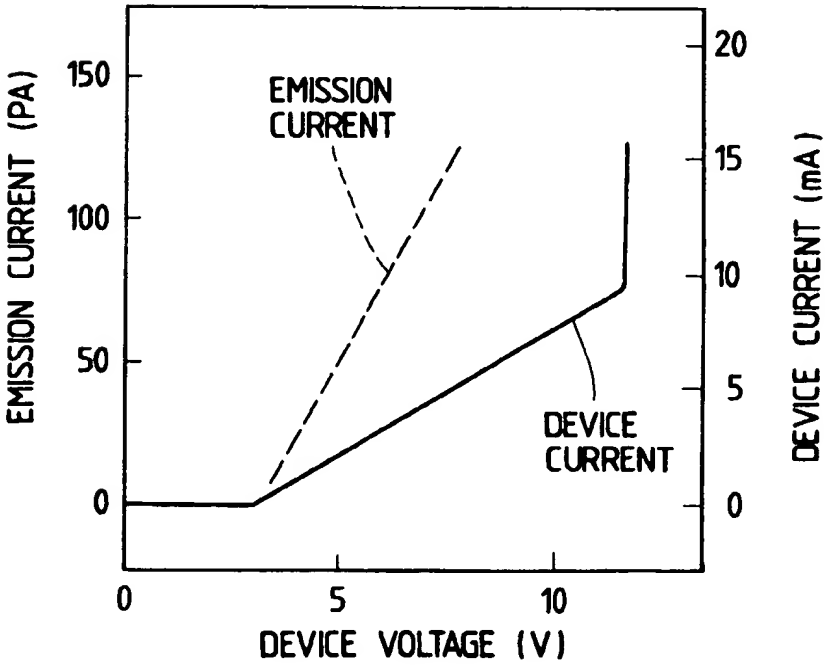

EMISSION CURRENT (PA)
150
100
50
0
EMISSION CURRENT
DEVICE CURRENT
20
15
10
5
0
DEVICE CURRENT (mA)
0
5
10
DEVICE VOLTAGE (V)

FIG. 5

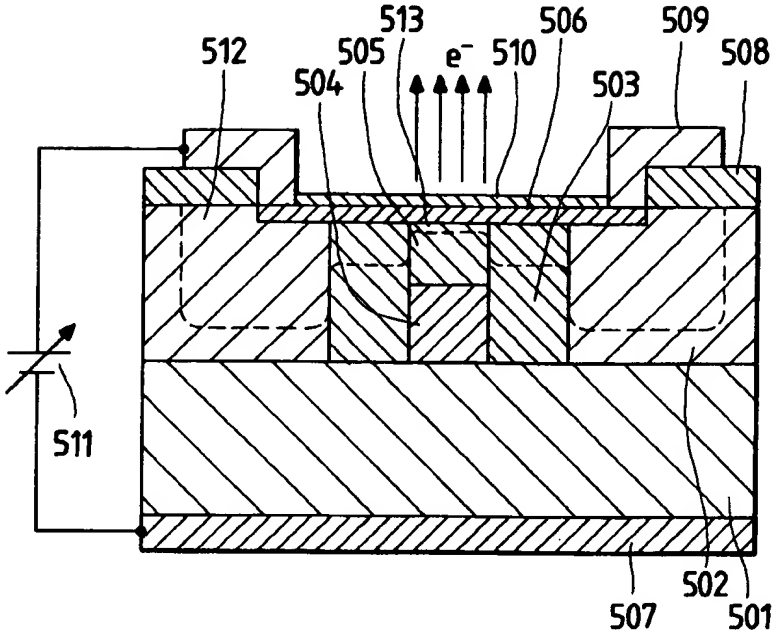

513
506
509
512
505
e⁻
510
508
504
503
511
502
507
501

FIG. 12

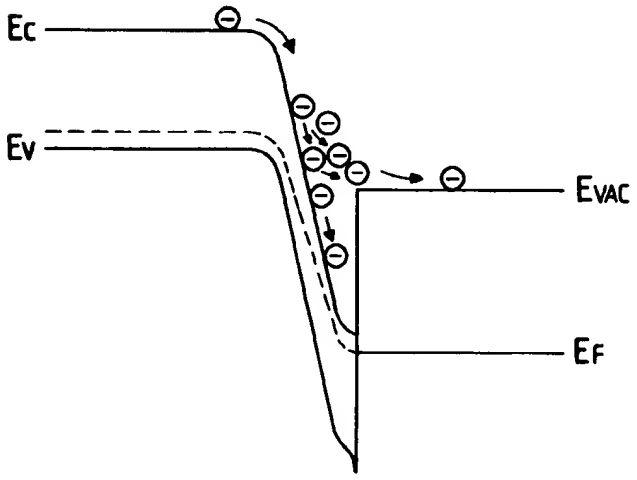

Ec
Ev
EVAC
EF

FIG. 6A

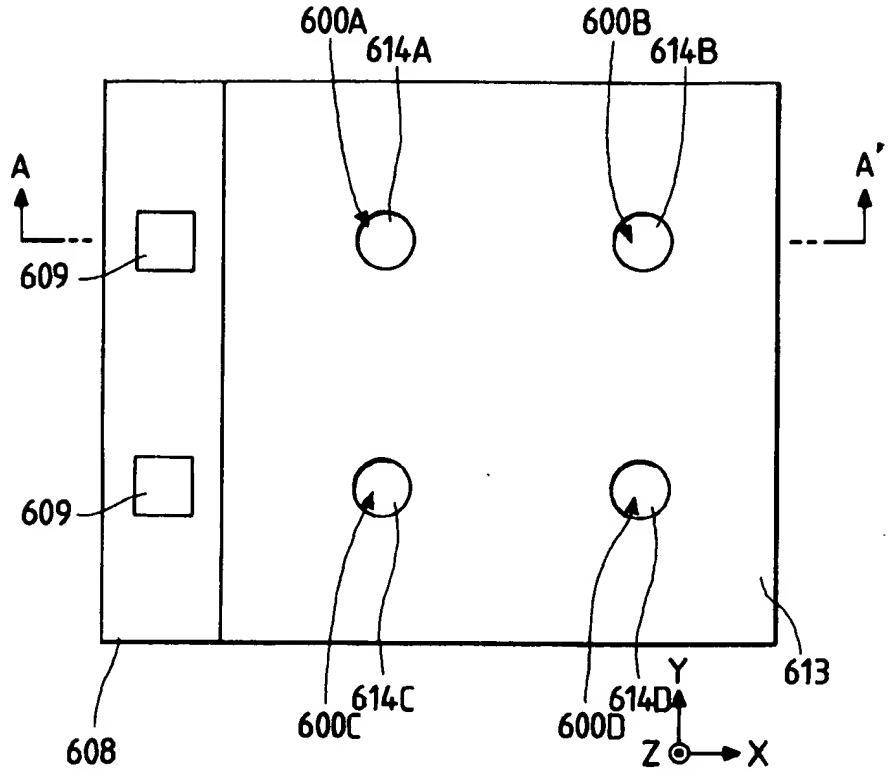

600A
614A
600B
614B
A
A'
609
609
613
608
600C
614C
600D
614D
Y
Z
X

FIG. 6B

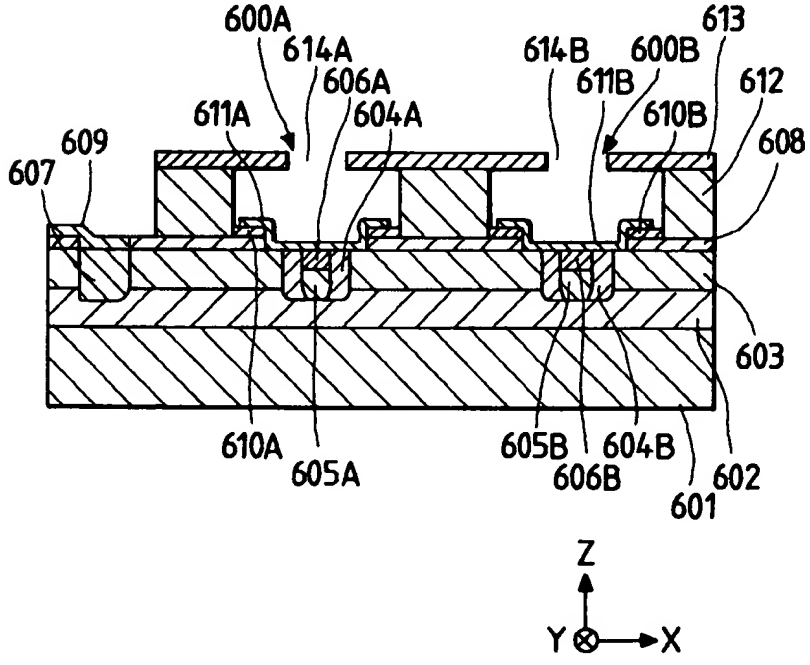

600A
614A
606A
611A
604A
614B
611B
600B
613
610B
612
609
607
608
603
610A
605A
605B
606B
604B
602
601
Z
Y
X

FIG. 7

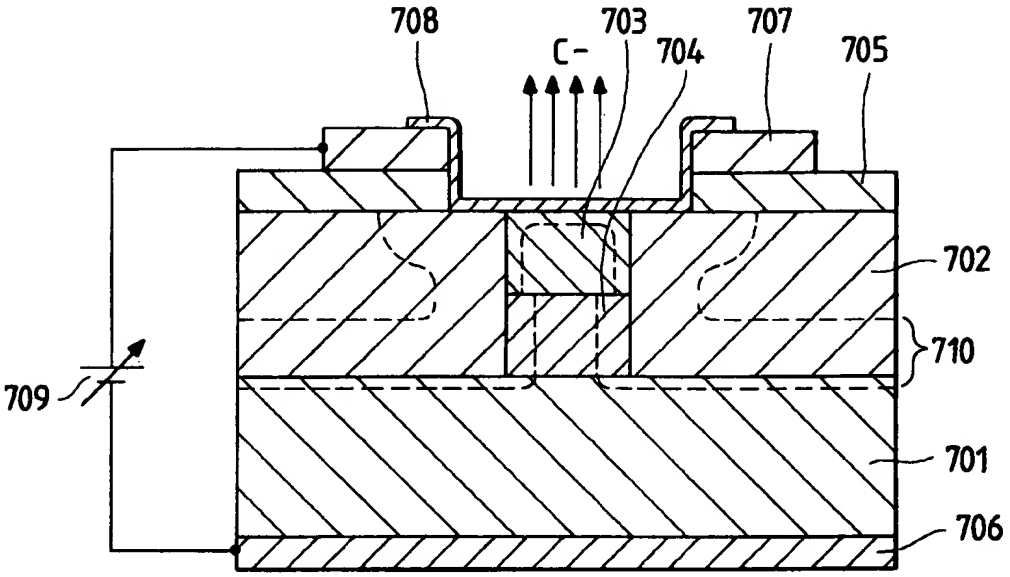

708
703
C-
704
707
705
702
710
709
701
706

FIG. 8

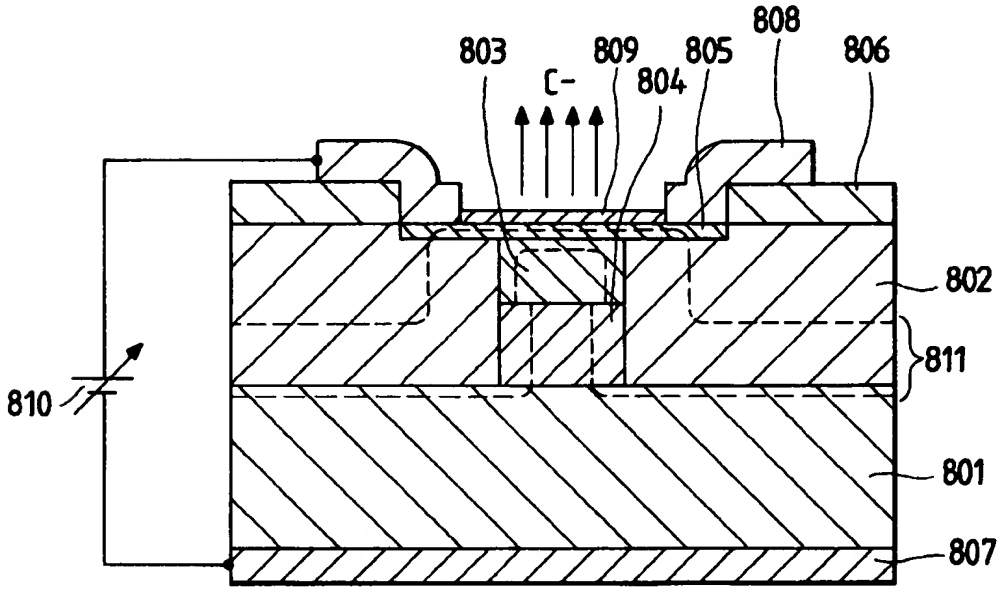

803
809
805
808
806
C-
804
802
811
810
801
807

FIG. 9A

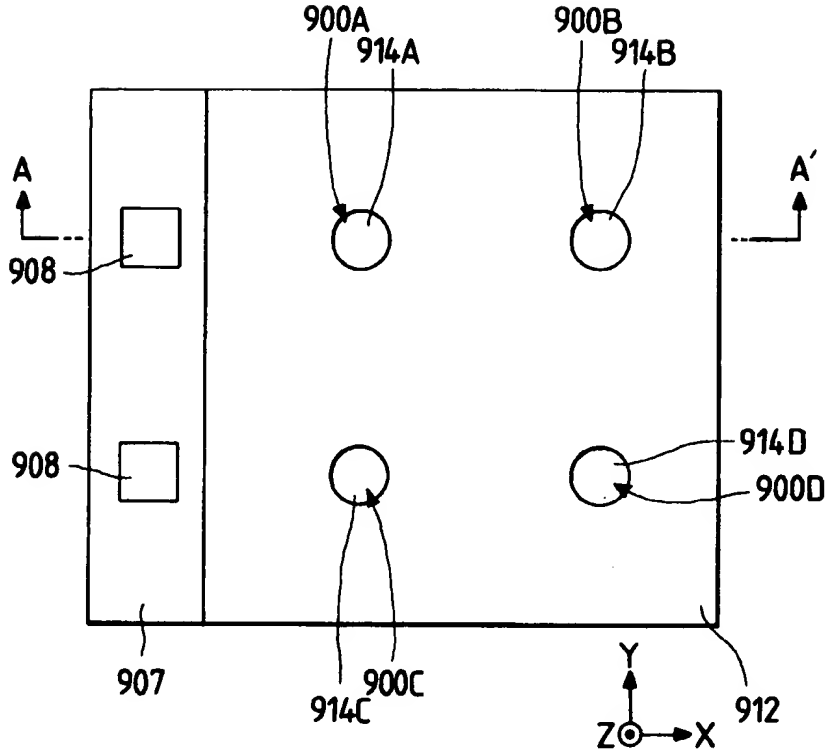

900A
914A
900B
914B
A
A'
908
908
914D
900D
907
914C
900C
912
Y
Z
X

FIG. 9B

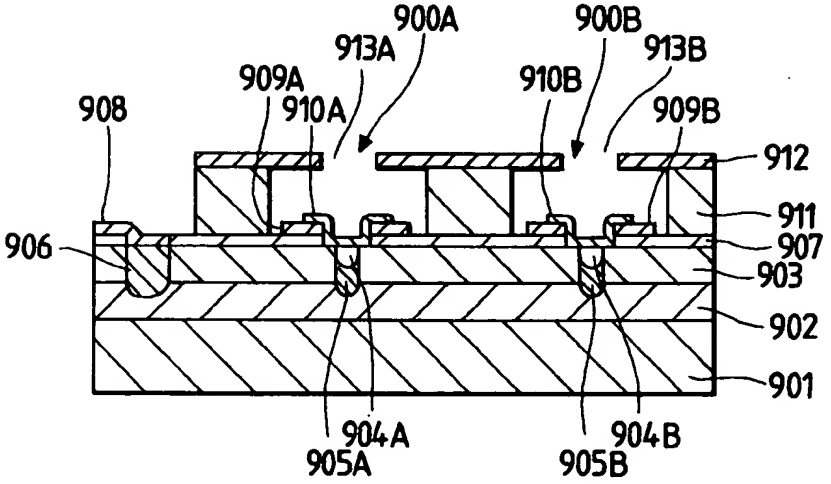

900A
913A
900B
913B
909A
910A
910B
909B
908
912
911
906
907
903
902
901
904A
905A
904B
905B

FIG. 10

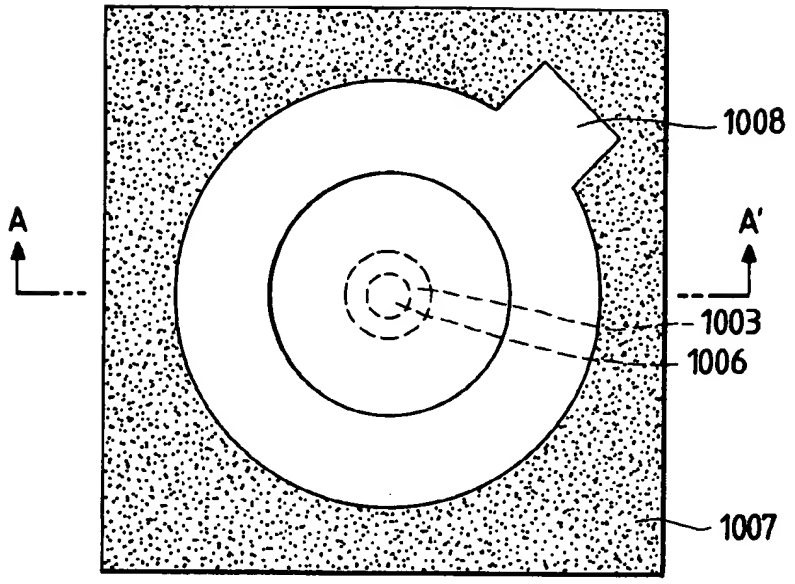

1008
A
A'
1003
1006
1007

FIG. 11

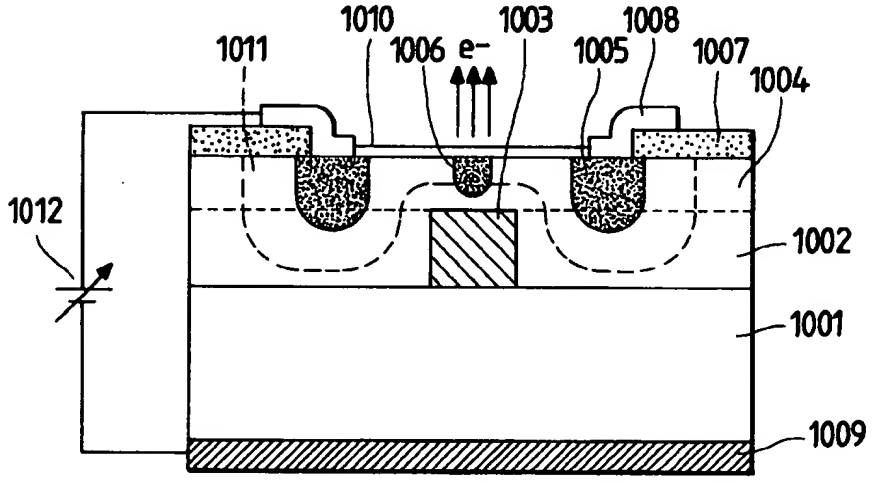

1010
1003
1008
1011
1006
e-
1005
1007
1004
1012
1002
1001
1009

FIG. 13

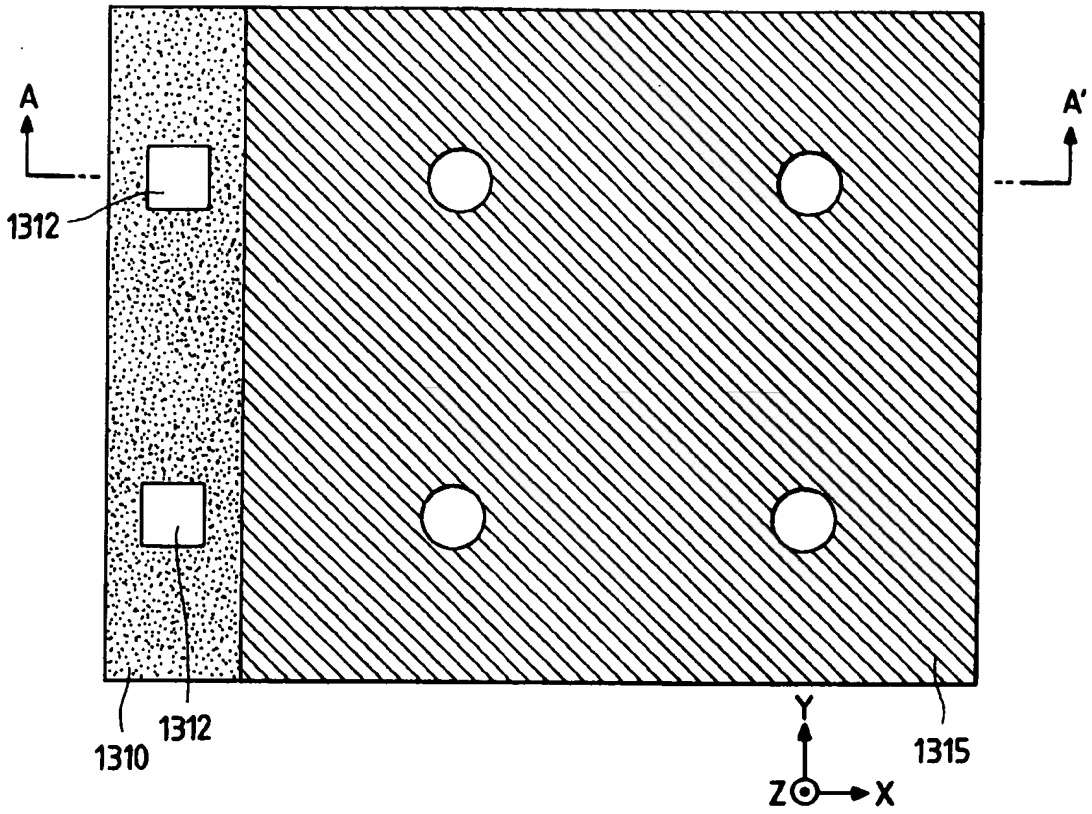

A
A'
1312
1310
1312
1315
Y
Z
X

FIG. 14

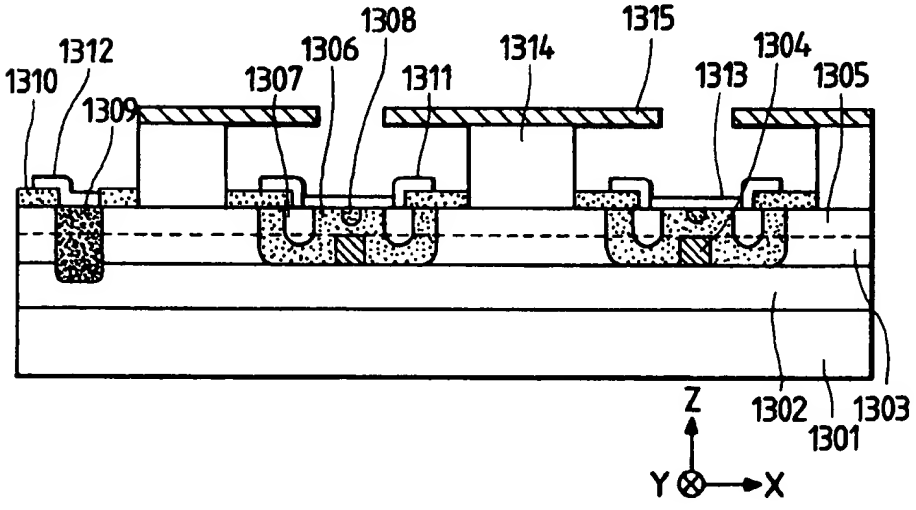

1310
1312
1309
1307
1306
1308
1311
1314
1315
1313
1304
1305
1302
1301
1303
Z
Y
X

FIG. 15A

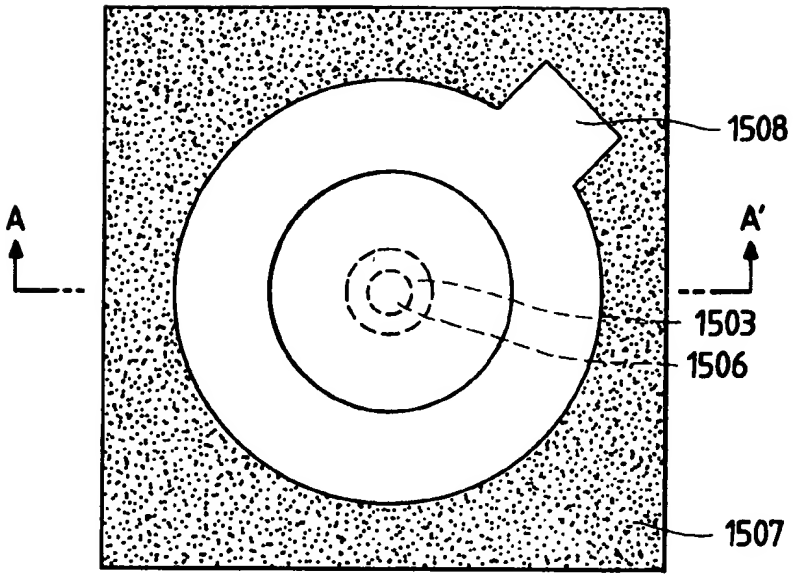


FIG. 15B

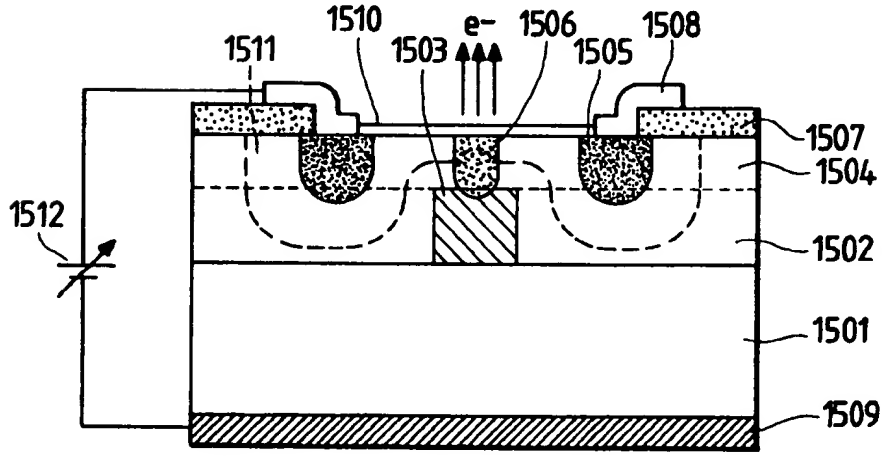


FIG. 16A

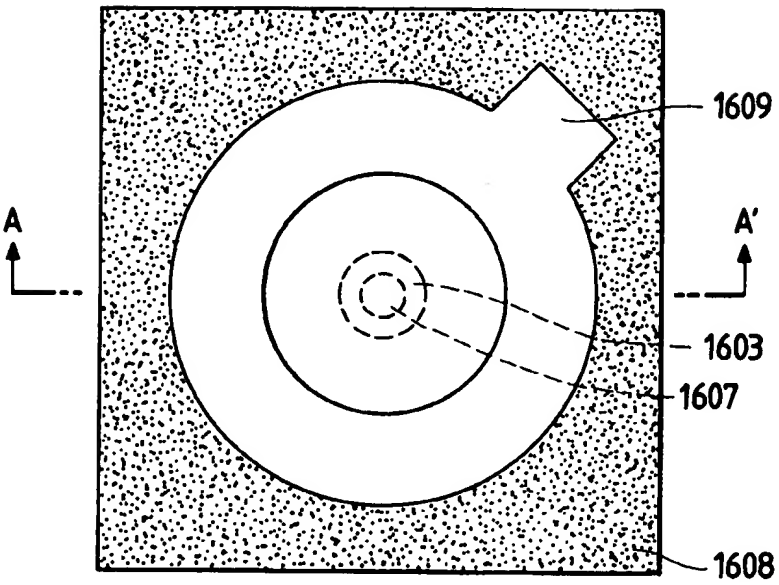


FIG. 16B

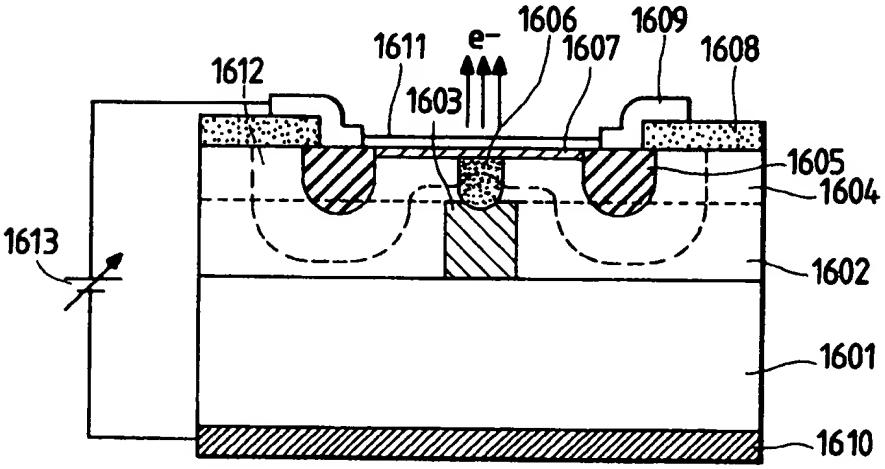


FIG. 17A

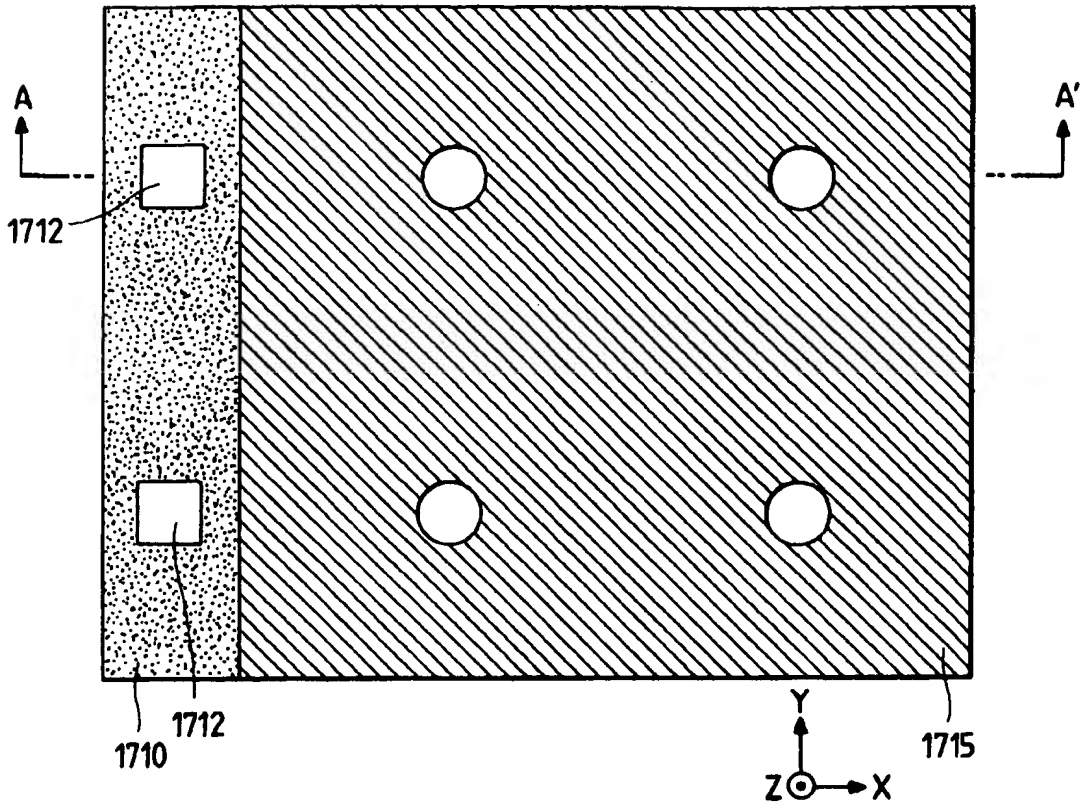


FIG. 17B